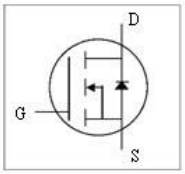
CT10NR009B

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

»Features

- Simple Driver Requirement
- Low On-resistance
- RoHS Compliant & Halogen-Free



BV_{DSS}	100V
$RDS(ON)_{Typ}$	8.1mΩ
I_D	50A

»Description

CT10NR009B is from Coretong innovated design and silicon process technology to achieve the lowest possible on- resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.

»Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	50	A
I_D@TC=100℃	Drain Current, V_{GS} @ 10V	31	A
I_{DM}	Pulsed Drain Current[1]	105	A
P_D@T_A=25℃	Total Power Dissipation	5	W
P_D@T_C=25℃	Total Power Dissipation	41.6	W
P_D@T_C=100℃	Total Power Dissipation	30	W
E_{AS}	Avalanche Energy, Single pulse[4]	15	mJ
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	150	℃

»Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	3	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	30	℃/W

»Electrical Characteristics@T_j=25 oC(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance2	V_{GS}=10V, I_D=20A	-	8.1	9.5	mΩ
		V_{GS}=4.5V, I_D=10A	-	11.4	14.5	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	2	3	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=20A	-	34	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V, V_{GS}=0V	-	-	1	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=20A V_{DS}=50V V_{GS}=10V	-	17	-	nC
Q_{gs}	Gate-Source Charge		-	5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	12	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50V I_D=1A R_G=3Ω V_{GS}=10V	-	16	-	ns
t_r	Rise Time		-	65	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	26	-	ns
t_f	Fall Time		-	51	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=50V f=1.0MHz	-	2550	-	pF
C_{oss}	Output Capacitance		-	1850	-	pF
Crss	Reverse Transfer Capacitance		-	575	-	pF
Rg	Gate Resistance	f=1.0MHz	-	1.1	-	Ω

»Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage2	I_S=20A, V_{GS}=0V	-	0.84	1.1	V
t_{rr}	Reverse Recovery Time	I_S=20A, V_R=50V dI/dt=100A/μs	-	49	-	ns
Q_{rr}	Reverse Recovery Charge		-	61	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse Test

3.Surface mounted on 1 in^2 2oz copper pad of FR4 board, t <10sec ; 60℃W when mounted on min. copper pad.

4.Starting Tj=25℃Vdd=50V,L=0.1mH,Rg=25Ω.

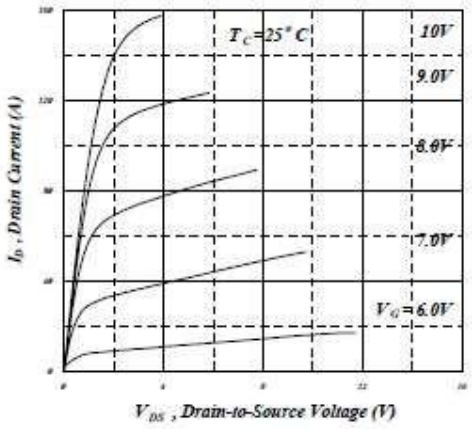


Fig 1. Typical Output Characteristics

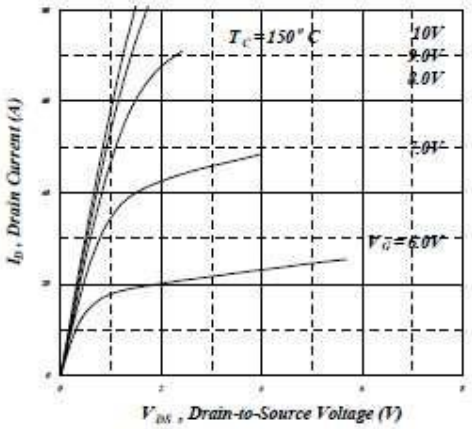


Fig 2. Typical Output Characteristics

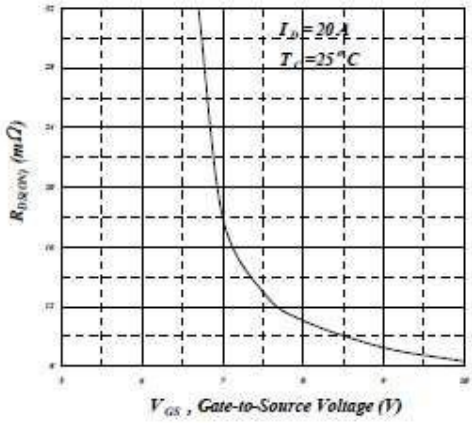


Fig 3. On-Resistance v.s. Gate Voltage

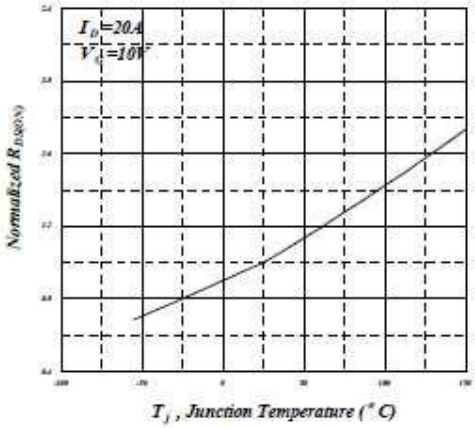


Fig 4. Normalized On-Resistance v.s. Junction Temperature

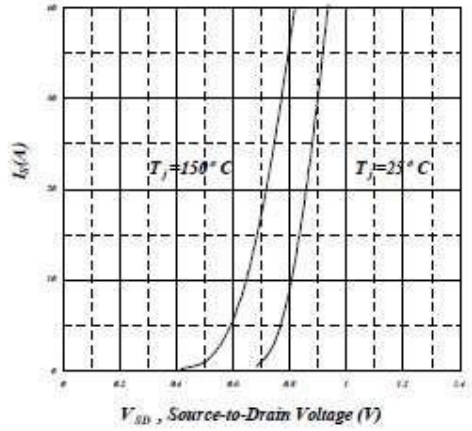


Fig 5. Forward Characteristic of Reverse Diode

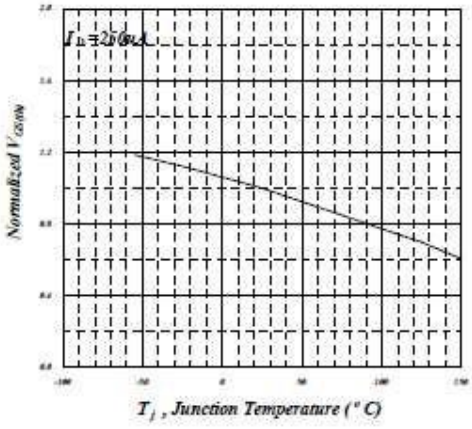


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

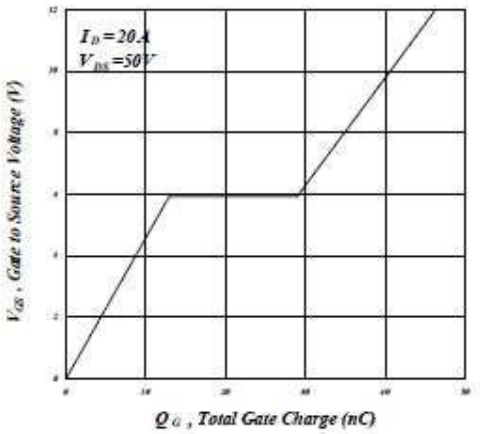


Fig 7. Gate Charge Characteristics

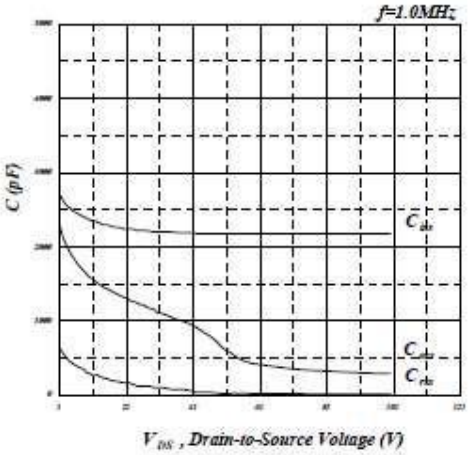


Fig 8. Typical Capacitance Characteristics

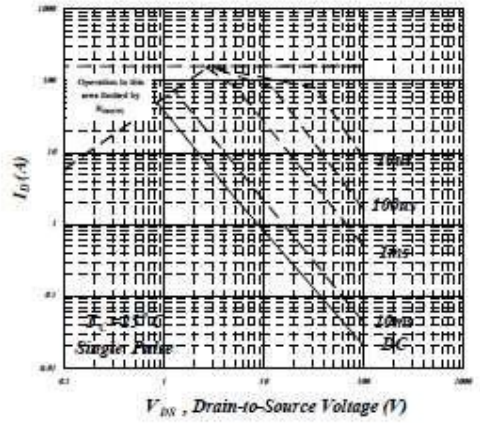


Fig 9. Maximum Safe Operating Area

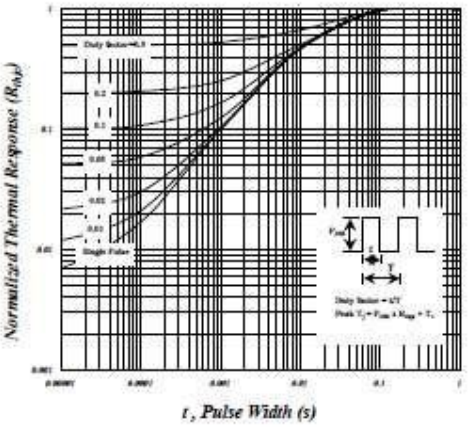


Fig 10. Effective Transient Thermal Impedance

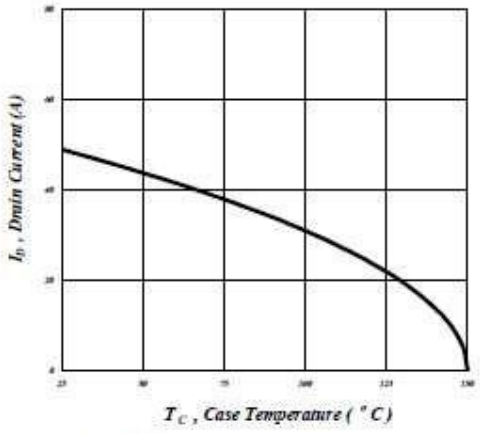


Fig 11. Drain Current v.s. Case Temperature

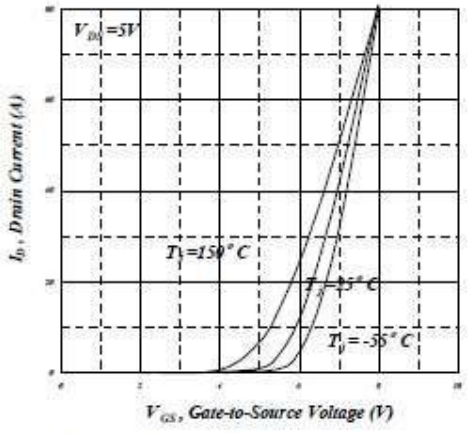


Fig 12. Transfer Characteristics

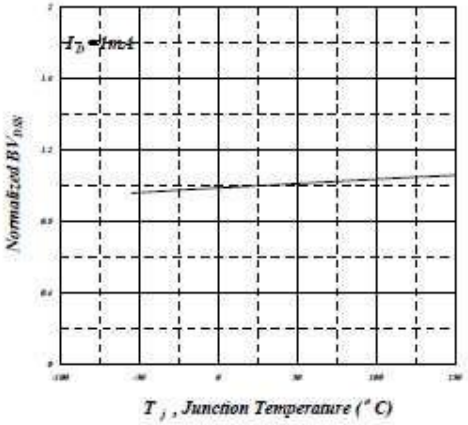


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

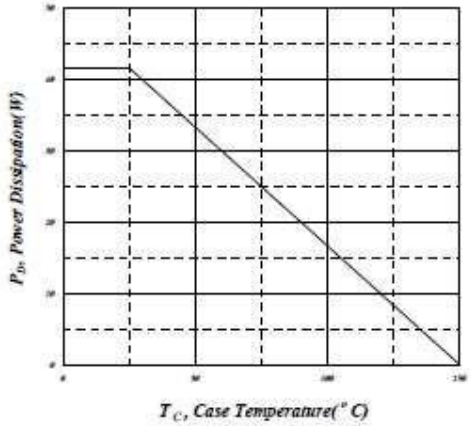


Fig 14. Total Power Dissipation

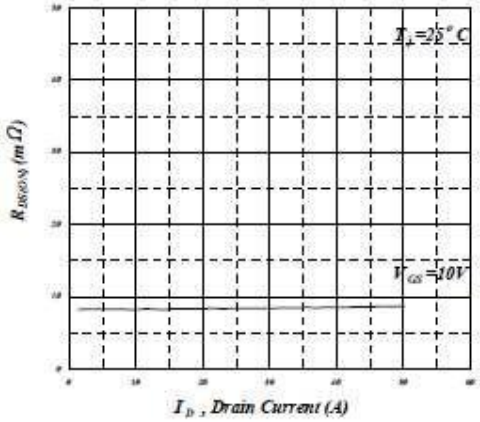


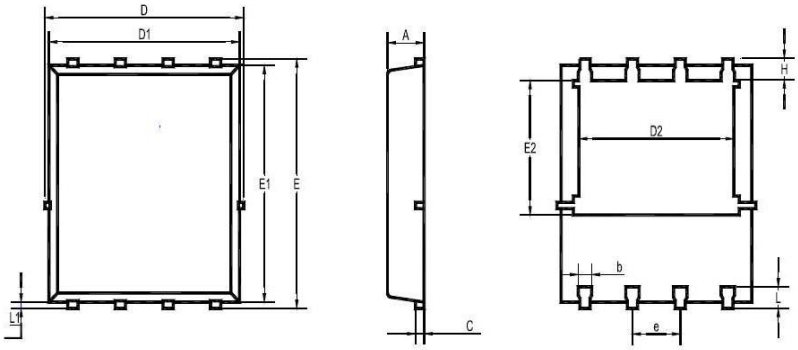
Fig 15. Typ. Drain-Source on State Resistance

»Marking Information

Package	PDFN5x6	
XXXX	Part Number	
Y	Year	F=2020 , G=2021, ……
WW	Weeks	Ex. 10/27=44weeks, 11/3=45weeks
FF	Wafer lot	Lot No.
A	Serial	Serial No.
Dot	First pin	

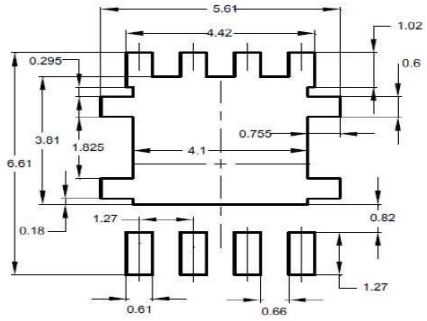
Package Outline Dimensions (Units: mm)

PDFN5x6



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12	0.51	0.34	5.26	5.1	4. 5	6.25	6	3.66	1.37	0.71	0.2	0.71
	0.9	0.33	0.11	4.7	4.7	3.56	5.75	5.6	3.18	1.17	0.35	0.06	0.35

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
PDFN5x6	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000