Linear Voltage Regulator - Ultra-Low Iq, Wide Input Voltage, Low Dropout

50 mA

NCP715

The NCP715 is 50 mA LDO Linear Voltage Regulator. It is a very stable and accurate device with ultra−low ground current consumption (4.7 μA over the full output load range) and a wide input voltage range (up to 24 V). The regulator incorporates several protection features such as Thermal Shutdown and Current Limiting.

Features

- Operating Input Voltage Range: 2.5 V to 24 V
- Fixed Voltage Options Available: 1.2 V to 5.3 V
- Ultra Low Quiescent Current: Max. 4.7 μA Over Full Load and Temperature
- ±2% Accuracy Over Full Load, Line and Temperature Variations
- PSRR: 52 dB at 100 kHz
- Noise: 190 μV_{RMS} from 200 Hz to 100 kHz
- Thermal Shutdown and Current Limit protection
- Available in XDFN6 1.5 x 1.5 mm, SC−70 (SC−88A) and TSOP−5 Packages
- These are Pb−Free Devices

Typical Applications

- Portable Equipment
- Communication Systems

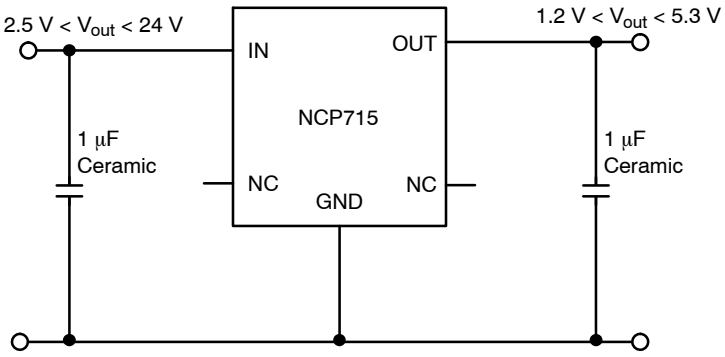
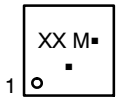


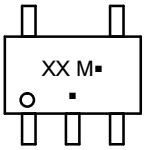
Figure 1. Typical Application Schematic

MARKING DIAGRAMS

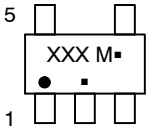
XDFN6
CASE 711AE



SC−70−5
(SC−88A)
CASE 419A



TSOP−5
CASE 483



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

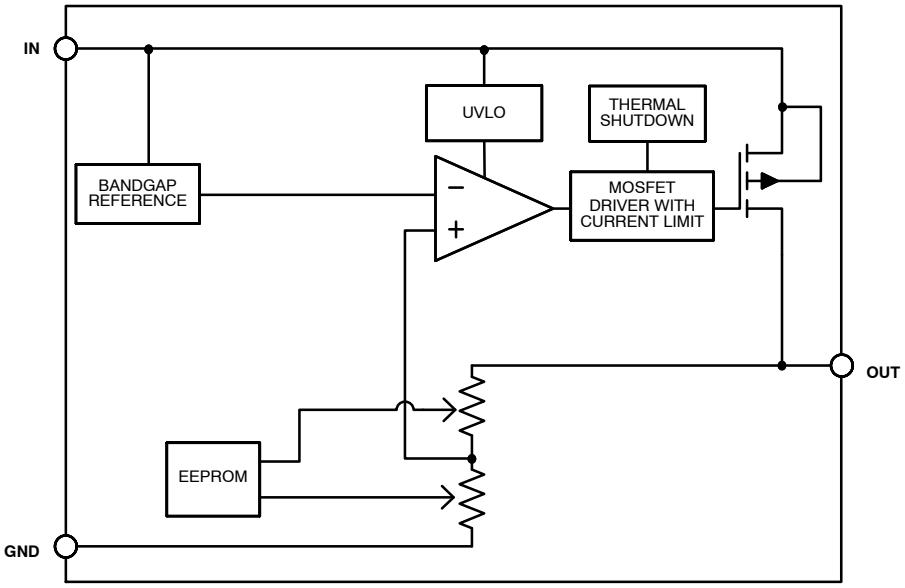


Figure 2. Simplified Block Diagram

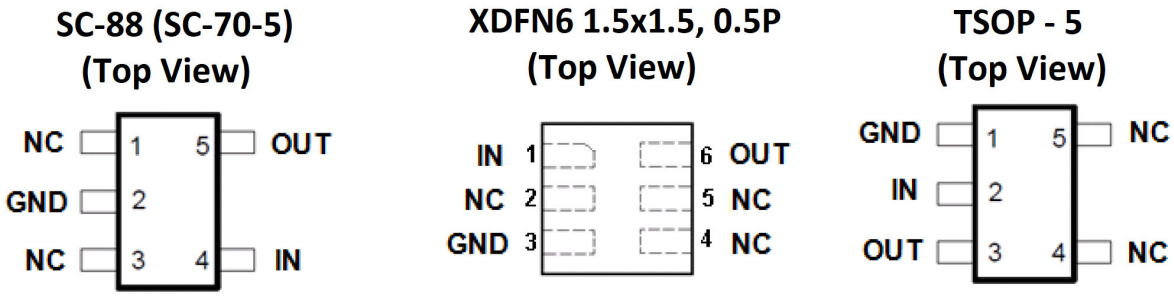


Figure 3. Pin Description

PIN FUNCTION DESCRIPTION

Pin No.			Pin Name	Description
SC−70	XDFN6	TSOP−5		
5	6	3	OUT	Regulated output voltage pin. A small 0.47 μF ceramic capacitor is needed from this pin to ground to assure stability.
1	2	4	N/C	No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected.
2	3	1	GND	Power supply ground.
3	4	5	N/C	No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected.
–	5	–	N/C	No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected.
4	1	2	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 24	V
Output Voltage	V_{OUT}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Operating Ambient Temperature Range	T_A	−40 to 125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   ESD Charged Device Model tested per EIA/JESD22−C101E
   Latch up Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SC−70 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	390	°C/W
Thermal Characteristics, XDFN6 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	260	°C/W
Thermal Characteristics, TSOP−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W

ELECTRICAL CHARACTERISTICS – Voltage Version 1.2 V

$-40°C \le T_J \le 125°C$; V_{IN} = 2.5 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$I_{OUT} \le 10$ mA	V_{IN}	2.5		24	V
	10 mA< I_{OUT} < 50 mA		3.0		24	
Output Voltage Accuracy	2.5 V < V_{IN} < 24 V, 0 < $I_{OUT} \le 10$ mA	V_{OUT}	1.164	1.2	1.236	V
	3.0 V < V_{IN} < 24 V, 0 mA < I_{OUT} < 50 mA	V_{OUT}	1.164	1.2	1.236	V
	3.0 V < V_{IN} < 24 V, 1 mA < I_{OUT} < 50 mA, −20°C < T_J < 125°C;	V_{OUT}	1.176	1.2	1.224	V
Line Regulation	2.5 V ≤ V_{IN} ≤ 24 V, I_{OUT} = 1 mA	Reg_{LINE}		2		mV
Load Regulation	I_{OUT} = 0 mA to 50 mA	Reg_{LOAD}		5		mV
Dropout Voltage (Note 3)		V_{DO}			–	mV
Maximum Output Current	(Note 6)	I_{OUT}	100		200	mA
	0 < I_{OUT} < 50 mA, −40 < T_A < 85°C	I_{GND}		3.2	4.2	μA
	0 < I_{OUT} < 50 mA, V_{IN} = 24 V				5.8	
Power Supply Rejection Ratio	V_{IN} = 3.0 V, V_{OUT} = 1.2 V, V_{PP} = 200 mV modulation, I_{OUT} = 1 mA, C_{OUT}= 10 μF, f = 100 kHz	PSRR		60		dB
Output Noise Voltage	V_{OUT} = 1.2 V, I_{OUT} = 50 mA, f = 200 Hz to 100 kHz, C_{OUT} = 10 μF	V_N		65		μV_{rms}
Thermal Shutdown Temperature (Note 4)	Temperature increasing from T_J = +25°C	T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 4)	Temperature falling from T_{SD}	T_{SDH}	–	15	–	°C

3. Not Characterized at V_{IN} = 3.0 V, V_{OUT} = 1.2 V, I_{OUT} = 50 mA.
4. Guaranteed by design and characterization.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. Respect SOA.

ELECTRICAL CHARACTERISTICS – Voltage Version 1.5 V

$-40°C \le T_J \le 125°C$; V_{IN} = 2.5 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 9)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$I_{OUT} \le 10$ mA	V_{IN}	2.5		24	V
	10 mA < I_{OUT} < 50 mA		3.0		24	
Output Voltage Accuracy	2.5 V < V_{IN} < 24 V, 0 < $I_{OUT} \le 10$ mA	V_{OUT}	1.455	1.5	1.545	V
	3.0 V < V_{IN} < 24 V, 0 < I_{OUT} < 50 mA	V_{OUT}	1.455	1.5	1.545	V
	3.0 V < V_{IN} < 24 V, 1 mA < I_{OUT} < 50 mA, −20°C < T_J < 125°C;	V_{OUT}	1.470	1.5	1.530	V
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, I_{OUT} = 1 mA	Reg_{LINE}		2		mV
Load Regulation	I_{OUT} = 0 mA to 50 mA	Reg_{LOAD}		5		mV
Dropout Voltage (Note 7)		V_{DO}			–	mV
Maximum Output Current	(Note 10)	I_{OUT}	100		200	mA
Ground Current	0 < I_{OUT} < 50 mA, −40 < T_A < 85°C	I_{GND}		3.2	4.2	μA
	0 < I_{OUT} < 50 mA, V_{IN} = 24 V				5.8	μA
Power Supply Rejection Ratio	V_{IN} = 3.0 V, V_{OUT} = 1.5 V, V_{PP} = 200 mV modulation, I_{OUT} = 1 mA, C_{OUT} = 10 μF; f = 100 kHz	PSRR		56		dB
Output Noise Voltage	V_{OUT} = 1.5 V, I_{OUT} = 50 mA, f = 200 Hz to 100 kHz, C_{OUT} = 10 μF	V_N		75		μV_{rms}
Thermal Shutdown Temperature (Note 8)	Temperature increasing from T_J = +25°C	T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 8)	Temperature falling from T_{SD}	T_{SDH}	–	15	–	°C

7. Not Characterized at V_{IN} = 3.0 V, V_{OUT} = 1.5 V, I_{OUT} = 50 mA.
8. Guaranteed by design and characterization.
9. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
10. Respect SOA.

ELECTRICAL CHARACTERISTICS – Voltage Version 1.8 V

$-40°C \le T_J \le 125°C$; V_{IN} = 2.8V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 13)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$I_{OUT} \le 10$ mA	V_{IN}	2.8		24	V
	10 mA < I_{OUT} < 50 mA		3.0		24	
Output Voltage Accuracy	2.8 V < V_{IN} < 24 V, 0 < I_{OUT} < 10 mA	V_{OUT}	1.746	1.8	1.854	V
	3.0 V < V_{IN} < 24 V, 1 mA < I_{OUT} < 50 mA, −20°C < T_J < 125°C;	V_{OUT}	1.764	1.8	1.836	V
Line Regulation	3 V ≤ V_{IN} ≤ 24 V, I_{OUT} = 1 mA	Reg_{LINE}		3		mV
Load Regulation	I_{OUT} = 0 mA to 50 mA	Reg_{LOAD}		10		mV
Dropout Voltage (Note 11)		V_{DO}				mV
Maximum Output Current	(Note 14)	I_{OUT}	100		200	mA
Ground Current	0 < I_{OUT} < 50 mA, −40 < T_A < 85°C	I_{GND}		3.2	4.2	μA
	0 < I_{OUT} < 50 mA, V_{IN} = 24 V				5.8	μA
Power Supply Rejection Ratio	V_{IN} = 3.0 V, V_{OUT} = 1.8 V, V_{PP} = 200 mV modulation, I_{OUT} = 1 mA, C_{OUT} =10 μF, f = 100 kHz	PSRR		60		dB
Output Noise Voltage	V_{OUT} = 1.8 V, I_{OUT} = 50 mA, f = 200 Hz to 100 kHz, C_{OUT} = 10 μF	V_N		95		μV_{rms}
Thermal Shutdown Temperature (Note 12)	Temperature increasing from T_J = +25°C	T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 12)	Temperature falling from T_{SD}	T_{SDH}	–	15	–	°C

11. Not characterized at V_{IN} = 3.0 V, V_{OUT} = 1.8 V, I_{OUT} = 50 mA
12. Guaranteed by design and characterization.
13. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
14. Respect SOA.

ELECTRICAL CHARACTERISTICS – Voltage Version 2.5 V

$-40°C \le T_J \le 125°C$; V_{IN} = 3.5 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 17)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$0 < I_{OUT} < 50$ mA	V_{IN}	3.5		24	V
Output Voltage Accuracy	$3.5\ V < V_{IN} < 24\ V$, $0 < I_{OUT} < 50$ mA	V_{OUT}	2.45	2.5	2.55	V
Line Regulation	$V_{OUT} + 1\ V \le V_{IN} \le 24\ V$, I_{OUT} = 1 mA	Reg_{LINE}		3		mV
Load Regulation	I_{OUT} = 0 mA to 50 mA	Reg_{LOAD}		10		mV
Dropout Voltage (Note 15)	$V_{DO} = V_{IN} - (V_{OUT(NOM)} - 75\ mV)$, I_{OUT} = 50 mA	V_{DO}		260	450	mV
Maximum Output Current	(Note 18)	I_{OUT}	100		200	mA
Ground Current	$0 < I_{OUT} < 50$ mA, $-40 < T_A < 85°C$	I_{GND}		3.2	4.2	μA
	$0 < I_{OUT} < 50$ mA, V_{IN} = 24 V				5.8	μA
Power Supply Rejection Ratio	V_{IN} = 3.5 V, V_{OUT} = 2.5 V, V_{PP} = 200 mV modulation, I_{OUT} = 1 mA, C_{OUT} =10 μF, f = 100 kHz	PSRR		60		dB
Output Noise Voltage	V_{OUT} = 2.5 V, I_{OUT} = 50 mA, f = 200 Hz to 100 kHz, C_{OUT} = 10 μF	V_N		115		μV_{rms}
Thermal Shutdown Temperature (Note 16)	Temperature increasing from T_J = +25°C	T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 16)	Temperature falling from T_{SD}	T_{SDH}	–	15	–	°C

15. Characterized when V_{OUT} falls 75 mV below the regulated voltage and only for devices with V_{OUT} = 2.5 V.
16. Guaranteed by design and characterization.
17. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
18. Respect SOA.

ELECTRICAL CHARACTERISTICS – Voltage Version 3.0 V

$-40°C \le T_J \le 125°C$; V_{IN} = 4.0 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 21)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$0 < I_{OUT} < 50$ mA	V_{IN}	4.0		24	V
Output Voltage Accuracy	4.0 V < V_{IN} < 24 V, 0< I_{OUT} < 50 mA	V_{OUT}	2.94	3.0	3.06	V
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, I_{OUT} = 1 mA	Reg_{LINE}		3		mV
Load Regulation	I_{OUT} = 0 mA to 50 mA	Reg_{LOAD}		10		mV
Dropout voltage (Note 19)	$V_{DO} = V_{IN} - (V_{OUT(NOM)} - 90$ mV) I_{OUT} = 50 mA	V_{DO}		250	400	mV
Maximum Output Current	(Note 22)	I_{OUT}	100		200	mA
Ground current	0 < I_{OUT} < 50 mA, -40 < T_A < 85°C	I_{GND}		3.2	4.2	μA
	0 < I_{OUT} < 50 mA, V_{IN} = 24 V				5.8	μA
Power Supply Rejection Ratio	V_{IN} = 4.0 V, V_{OUT} = 3.0 V, V_{PP} = 100 mV modulation, I_{OUT} = 1 mA, C_{OUT} = 10 μF, f = 100 kHz	PSRR		60		dB
Output Noise Voltage	V_{OUT} = 3 V, I_{OUT} = 50 mA, f = 200 Hz to 100 kHz, C_{OUT} = 10 μF	V_N		135		μV_{rms}
Thermal Shutdown Temperature (Note 20)	Temperature increasing from T_J = +25°C	T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 20)	Temperature falling from T_{SD}	T_{SDH}	-	25	-	°C

19. Characterized when V_{OUT} falls 90 mV below the regulated voltage and only for devices with V_{OUT} = 3.0 V
20. Guaranteed by design and characterization.
21. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
22. Respect SOA

ELECTRICAL CHARACTERISTICS – Voltage Version 3.3 V

$-40°C \le T_J \le 125°C$; V_{IN} = 4.3 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 25)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$0 < I_{OUT} < 50$ mA	V_{IN}	4.3		24	V
Output Voltage Accuracy	4.3 V < V_{IN} < 24 V, $0 < I_{OUT} < 50$ mA	V_{OUT}	3.234	3.3	3.366	V
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, I_{OUT} = 1 mA	Reg_{LINE}		3	10	mV
Load Regulation	I_{OUT} = 0 mA to 50 mA	Reg_{LOAD}		10		mV
Dropout Voltage (Note 23)	$V_{DO} = V_{IN} - (V_{OUT(NOM)} - 99$ mV) I_{OUT} = 50 mA	V_{DO}		230	350	mV
Maximum Output Current	(Note 26)	I_{OUT}	100		200	mA
Ground Current	$0 < I_{OUT} < 50$ mA, $-40 < T_A < 85°C$	I_{GND}		3.2	4.2	μA
	$0 < I_{OUT} < 50$ mA, V_{IN} = 24 V				5.8	μA
Power Supply Rejection Ratio	V_{IN} = 4.3 V, V_{OUT} = 3.3 V, V_{PP} = 200 mV modulation, I_{OUT} = 1 mA, C_{OUT} =10 μF, f = 100 kHz	PSRR		60		dB
Output Noise Voltage	V_{OUT} = 4.3 V, I_{OUT} = 50 mA f = 200 Hz to 100 kHz, C_{OUT} = 10 μF	V_N		140		μV_{rms}
Thermal Shutdown Temperature (Note 24)	Temperature increasing from T_J = +25°C	T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 24)	Temperature falling from T_{SD}	T_{SDH}	–	15	–	°C

23. Characterized when V_{OUT} falls 99 mV below the regulated voltage and only for devices with V_{OUT} = 3.3 V.
24. Guaranteed by design and characterization.
25. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
26. Respect SOA.

ELECTRICAL CHARACTERISTICS – Voltage Version 5.0 V

$-40°C \le T_J \le 125°C$; V_{IN} = 6.0 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 29)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	0 < I_{OUT} < 50 mA	V_{IN}	6.0		24	V
Output Voltage Accuracy	6.0V < V_{IN} < 24V, 0< I_{OUT} < 50 mA	V_{OUT}	4.9	5.0	5.1	V
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, Iout = 1mA	Reg_{LINE}		3	10	mV
Load Regulation	I_{OUT} = 0 mA to 50 mA	Reg_{LOAD}		10	30	mV
Dropout Voltage (Note 27)	V_{DO} = V_{IN} – ($V_{OUT(NOM)}$ – 150 mV) I_{OUT} = 50 mA	V_{DO}		230	350	mV
Maximum Output Current	(Note 30)	I_{OUT}	90		200	mA
Ground Current	0 < I_{OUT} < 50 mA, –40 < T_A < 85°C	I_{GND}		3.2	4.2	μA
	0 < I_{OUT} < 50 mA, V_{IN} = 24 V				5.8	μA
Power Supply Rejection Ratio	V_{IN} = 6.0 V, V_{OUT} = 5.0 V, f = 100 kHz V_{PP} = 200 mV modulation I_{OUT} = 1 mA, C_{OUT} =10 μF	PSRR		56		dB
Output Noise Voltage	V_{OUT} = 5.0 V, I_{OUT} = 50 mA f = 200 Hz to 100 kHz, C_{OUT} = 10 μF	V_N		190		μV_{rms}
Thermal Shutdown Temperature (Note 28)	Temperature increasing from T_J = +25°C	T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 28)	Temperature falling from T_{SD}	T_{SDH}	–	15	–	°C

27. Characterized when V_{OUT} falls 150 mV below the regulated voltage and only for devices with V_{OUT} = 5.0 V.
28. Guaranteed by design and characterization.
29. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
30. Respect SOA.

ELECTRICAL CHARACTERISTICS – Voltage Version 5.3 V

$-40°C \le T_J \le 125°C$; V_{IN} = 6.3 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 33)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$0 < I_{OUT} < 50$ mA	V_{IN}	6.3		24	V
Output Voltage Accuracy	$6.3V < V_{IN} < 24V$, 0.1 mA$< I_{OUT} < 50$ mA	V_{OUT}	5.194	5.3	5.406	V
Line Regulation	V_{OUT} + 1 V $\le V_{IN} \le$ 24 V, I_{OUT} = 1mA	Reg_{LINE}		20	60	mV
Load Regulation	I_{OUT} = 0.1 mA to 50 mA	Reg_{LOAD}		20		mV
Dropout Voltage (Note 31)	$V_{DO} = V_{IN} - (V_{OUT(NOM)} - 159$ mV) I_{OUT} = 50 mA	V_{DO}		230	350	mV
Maximum Output Current	(Note 34)	I_{OUT}	90		200	mA
Ground Current	$0 < I_{OUT} < 50$ mA, $-40 < T_A < 85°C$	I_{GND}		3.2	4.2	μA
	$0 < I_{OUT} < 50$ mA, V_{IN} = 24 V				5.8	μA
Power Supply Rejection Ratio	V_{IN} = 6.3 V, V_{OUT} = 5.3 V, V_{PP} = 200 mV modulation, I_{OUT} = 1 mA, C_{OUT} =10 μF, f = 100 kHz	PSRR		55		dB
Output Noise Voltage	V_{OUT} = 5.3 V, I_{OUT} = 50 mA f = 200 Hz to 100 kHz, C_{OUT} = 10 μF	V_N		195		μV_{rms}
Thermal Shutdown Temperature (Note 32)	Temperature increasing from T_J = +25°C	T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 32)	Temperature falling from T_{SD}	T_{SDH}	–	15	–	°C

31. Characterized when V_{OUT} falls 159 mV below the regulated voltage and only for devices with V_{OUT} = 5.3 V.
32. Guaranteed by design and characterization.
33. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
34. Respect SOA.

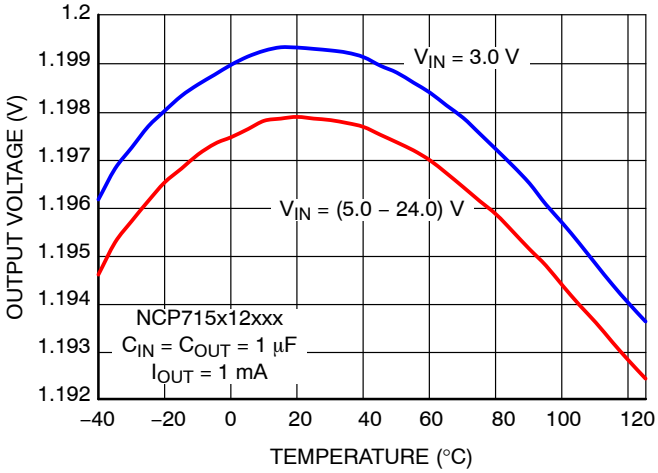


Figure 4. Output Voltage vs. Temperature

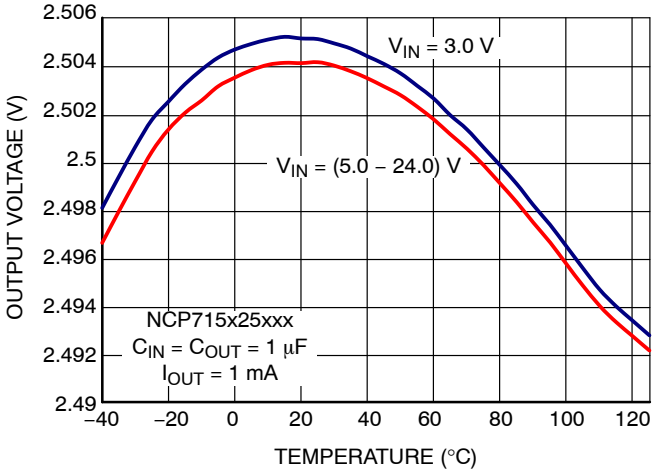


Figure 5. Output Voltage vs. Temperature

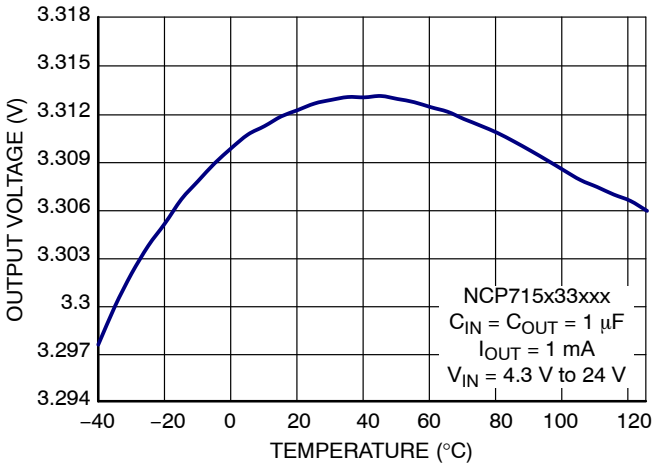


Figure 6. Output Voltage vs. Temperature

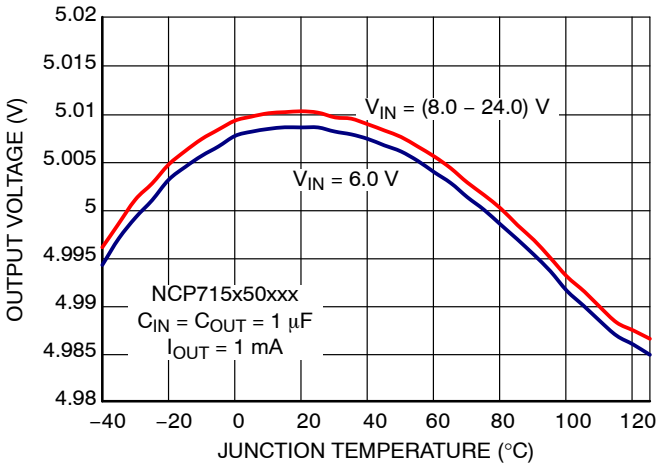


Figure 7. Output Voltage vs. Temperature

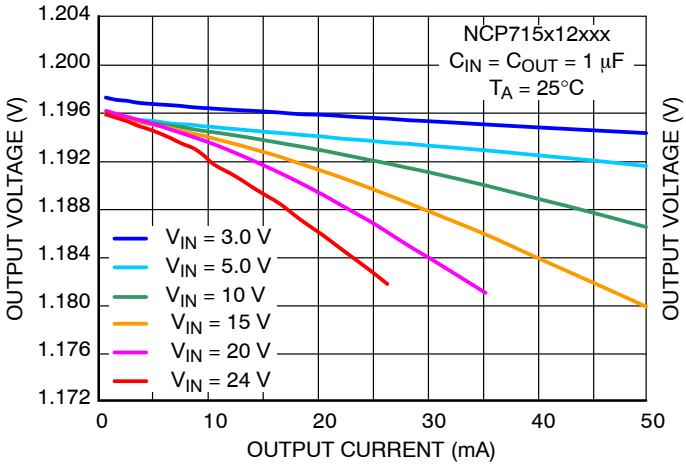


Figure 8. Output Voltage vs. Output Current

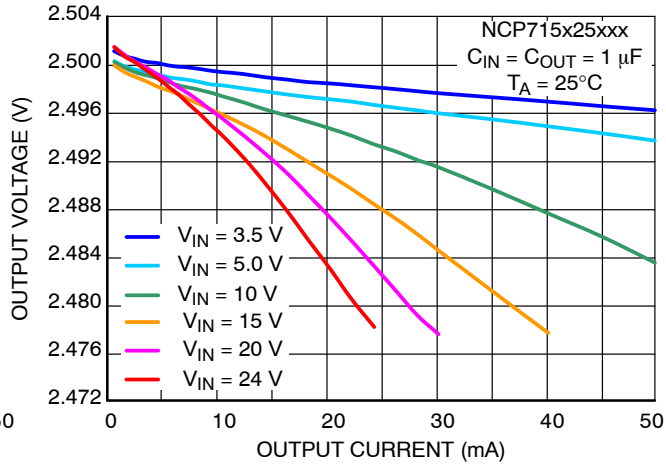


Figure 9. Output Voltage vs. Output Current

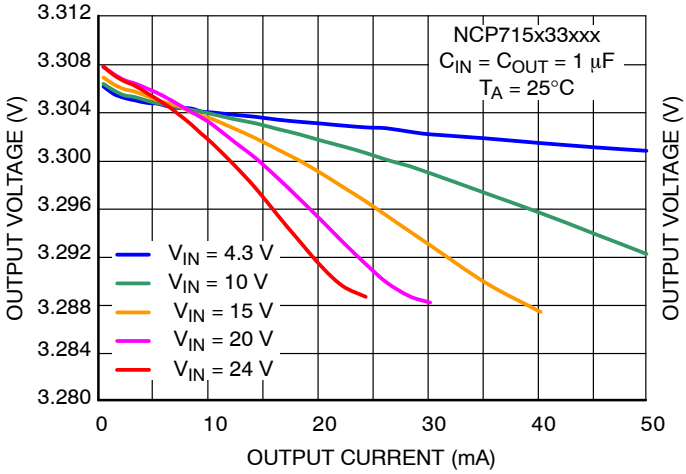


Figure 10. Output Voltage vs. Output Current

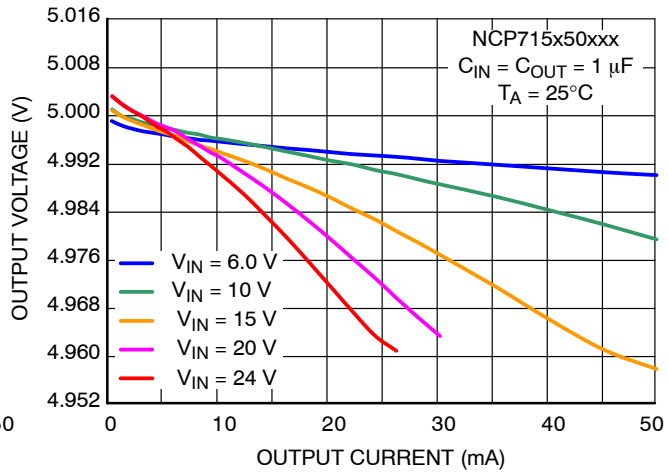


Figure 11. Output Voltage vs. Output Current

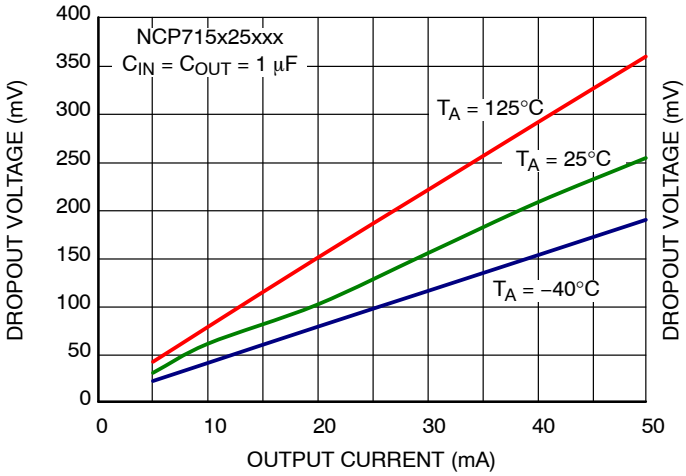


Figure 12. Dropout Voltage vs. Output Current

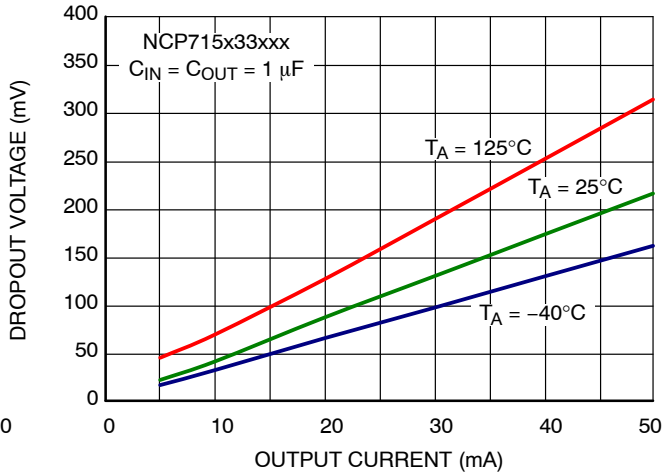


Figure 13. Dropout Voltage vs. Output Current

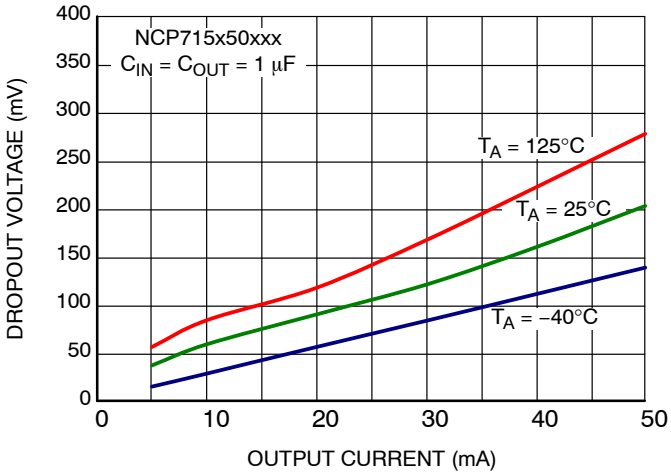


Figure 14. Dropout Voltage vs. Output Current

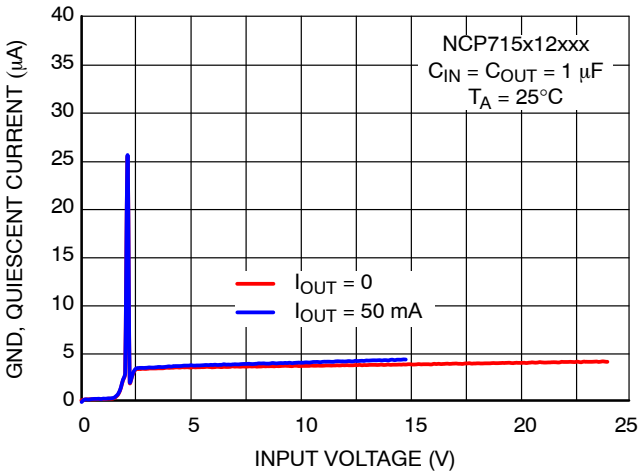


Figure 15. Ground Current vs. Input Voltage

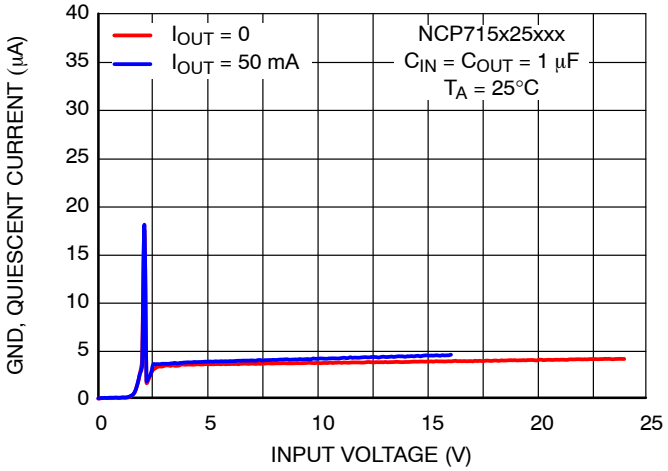


Figure 16. Ground Current vs. Input Voltage

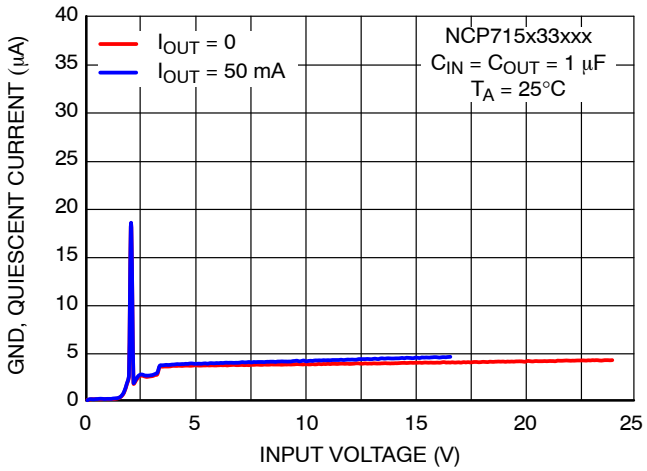


Figure 17. Ground Current vs. Input Voltage

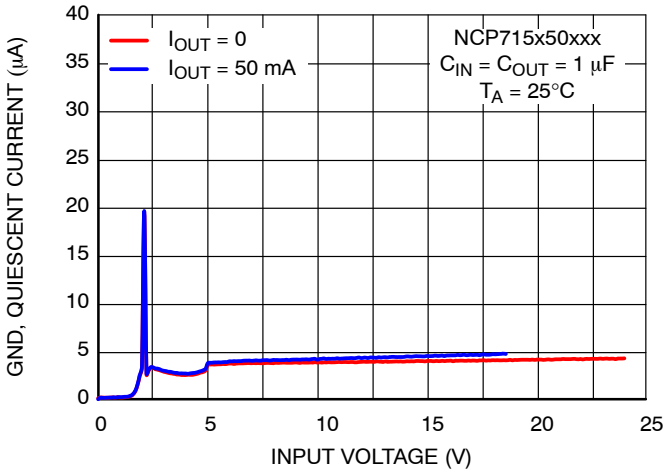


Figure 18. Ground Current vs. Input Voltage

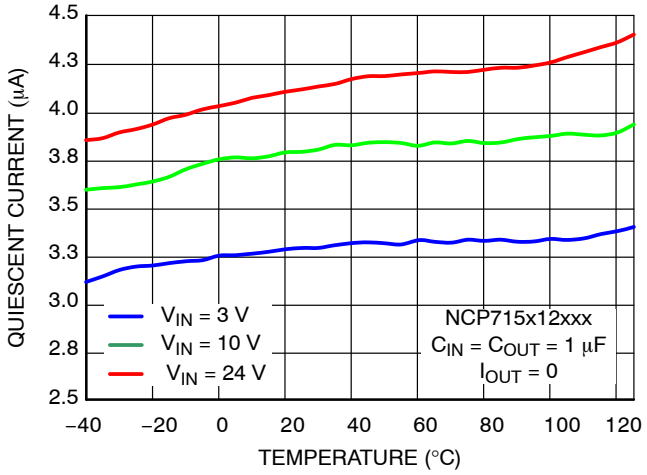


Figure 19. Quiescent Current vs. Temperature

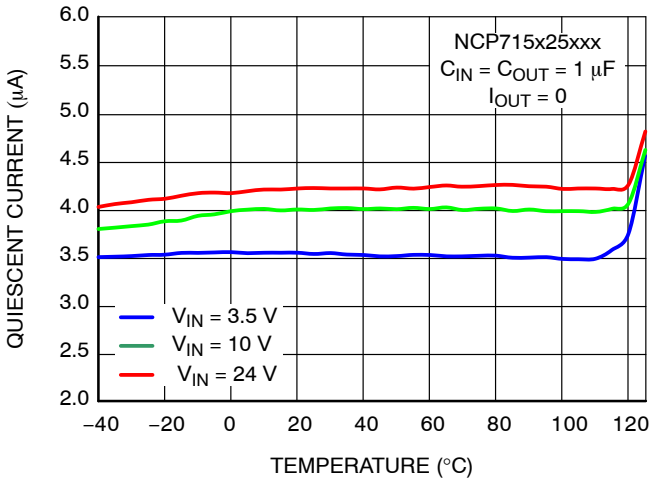


Figure 20. Quiescent Current vs. Temperature

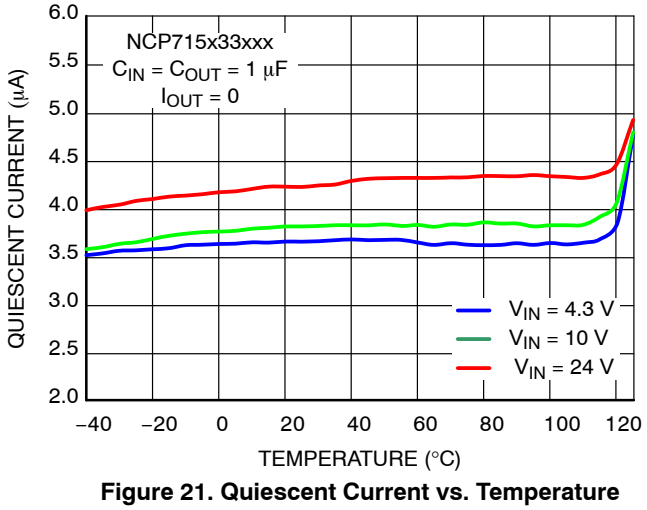


Figure 21. Quiescent Current vs. Temperature

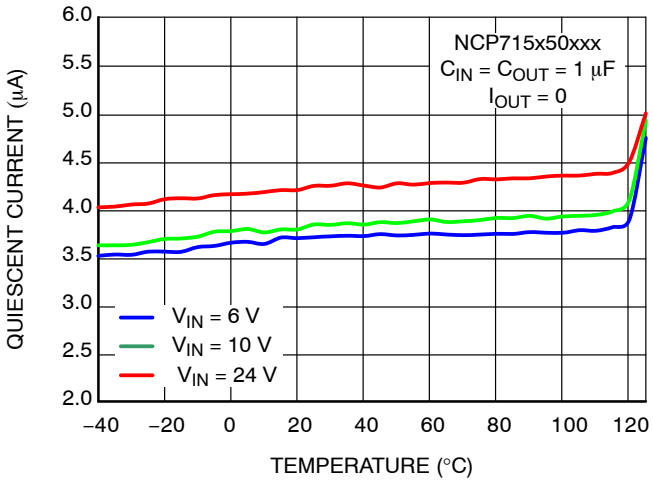


Figure 22. Quiescent Current vs. Temperature

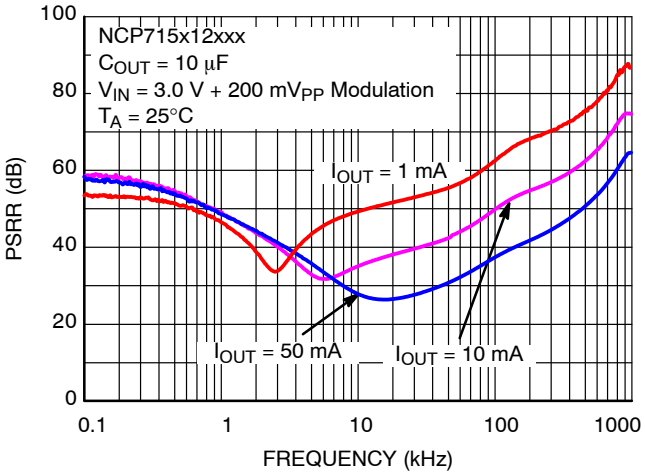


Figure 23. PSRR vs. Frequency

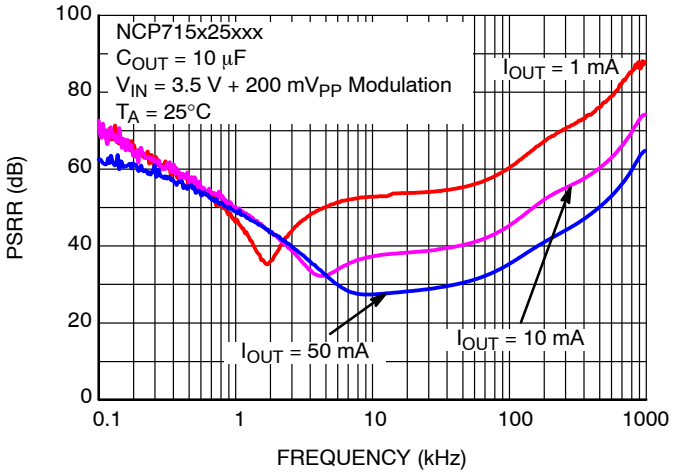


Figure 24. PSRR vs. Frequency

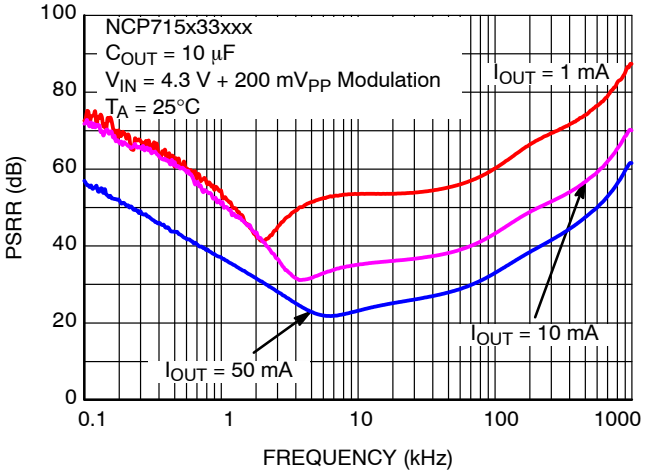


Figure 25. PSRR vs. Frequency

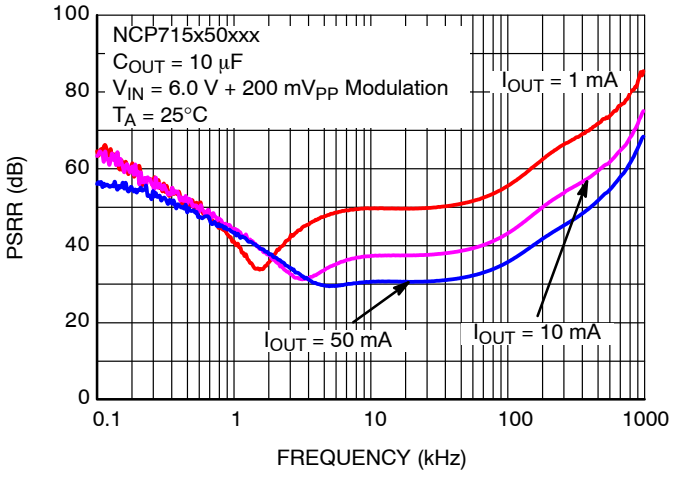


Figure 26. PSRR vs. Frequency

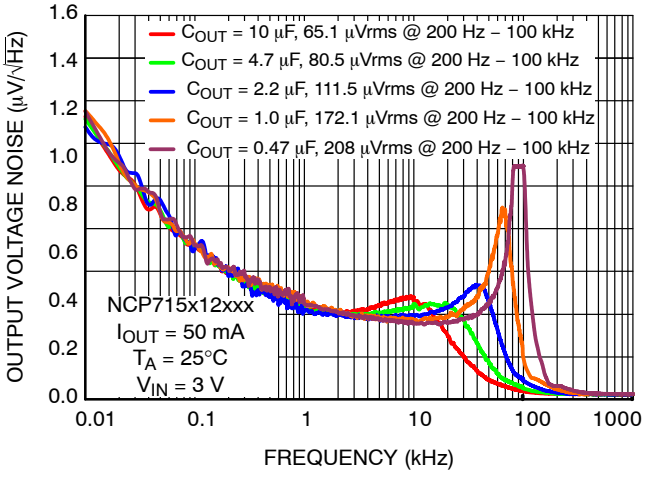


Figure 27. Output Spectral Noise Density vs. Frequency

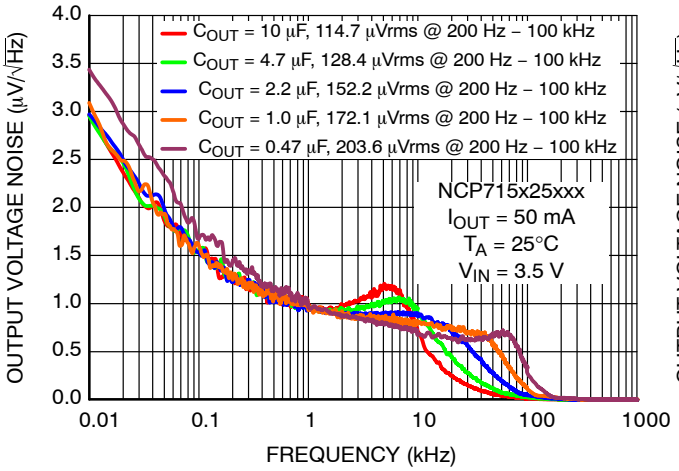


Figure 28. Output Spectral Noise Density vs. Frequency

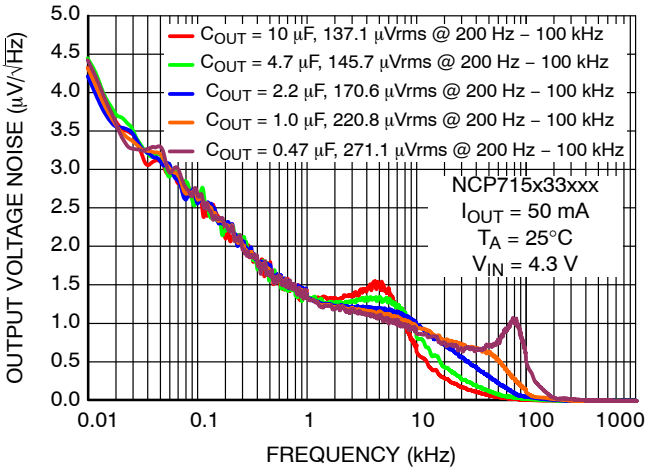


Figure 29. Output Spectral Noise Density vs. Frequency

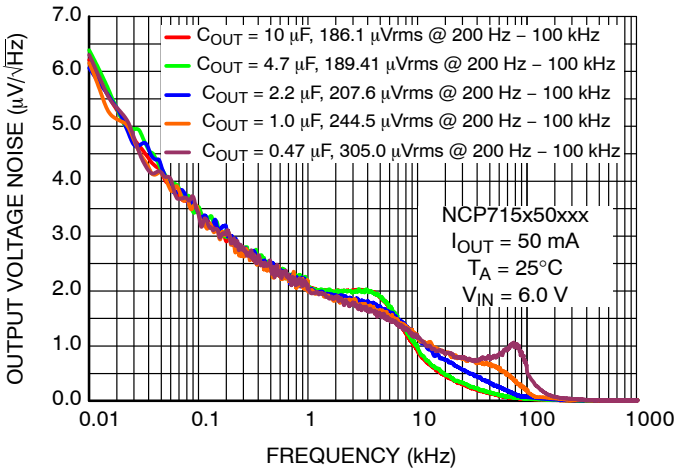


Figure 30. Output Spectral Noise Density vs. Frequency

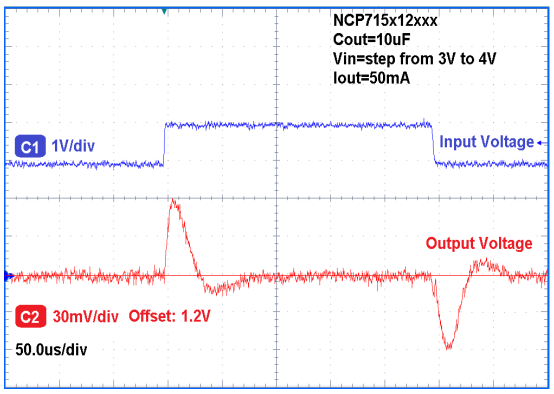


Figure 31. Line Transient Response

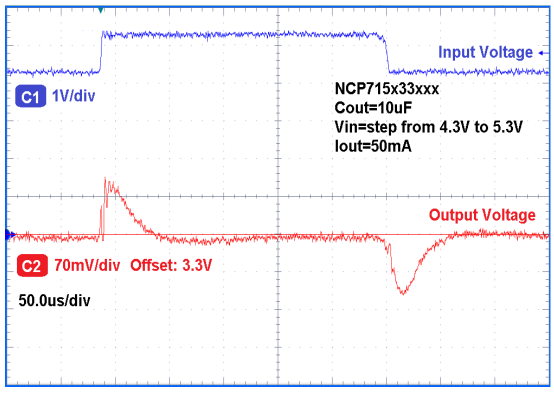


Figure 32. Line Transient Response

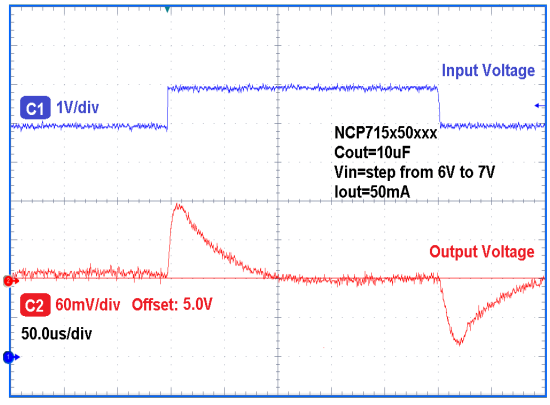


Figure 33. Line Transient Response

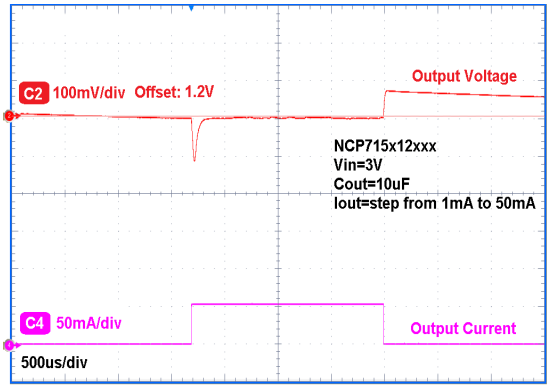


Figure 34. Load Transient Response

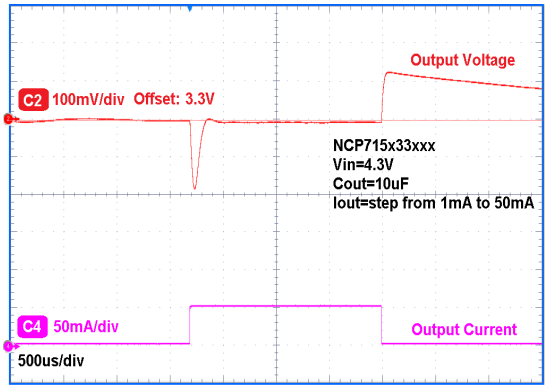


Figure 35. Load Transient Response

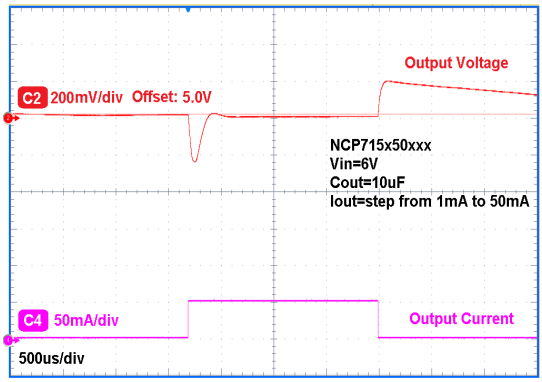


Figure 36. Load Transient Response

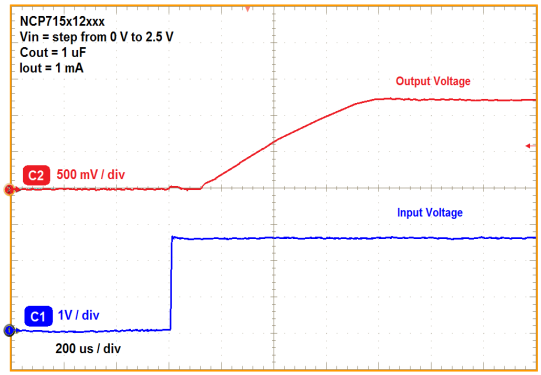


Figure 37. Input Voltage Turn−On Response

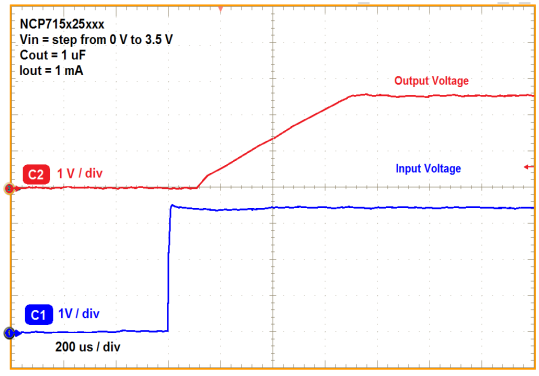


Figure 38. Input Voltage Turn−On Response

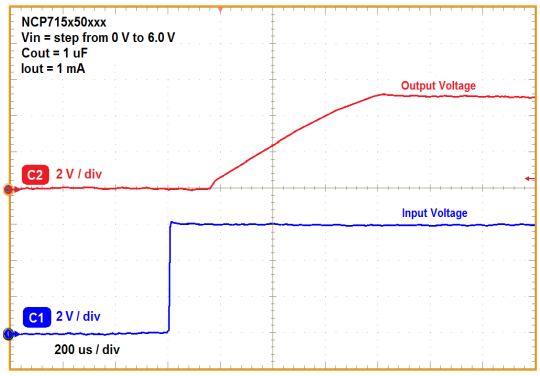


Figure 39. Input Voltage Turn−On Response

APPLICATIONS INFORMATION

The NCP715 is the member of new family of Wide Input Voltage Range Low Dropout Regulators which delivers Ultra Low Ground Current consumption, Good Noise and Power Supply Rejection Ratio Performance.

Input Decoupling (C_{IN})

It is recommended to connect at least 0.1 μF Ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or Noise superimposed onto constant Input Voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes.

Higher capacitance and lower ESR Capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCP715 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 0.47 μF or greater up to 10 μF. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

Power Dissipation and Heat sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the NCP715 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP715 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}\left(I_{OUT}\right)\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \quad \text{(eq. 3)}$$

For reliable operation, junction temperature should be limited to +125°C maximum.

Hints

VIN and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP715, and make traces as short as possible.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Marking Rotation	Package	Shipping†
NCP715SQ12T2G	1.2 V	5A	–	SC88A/SC70 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 35)
NCP715SQ15T2G	1.5 V	5C			
NCP715SQ18T2G	1.8 V	5D			
NCP715SQ25T2G	2.5 V	5E			
NCP715SQ30T2G	3.0 V	5F			
NCP715SQ33T2G	3.3 V	5G			
NCP715SQ50T2G	5.0 V	5H			
NCP715MX12TBG	1.2 V	Q	0°	XDFN6 1.5 x 1.5 (Pb−Free)	
NCP715MX15TBG (Note 35)	1.5 V	R			
NCP715MX18TBG (Note 35)	1.8 V	T			
NCP715MX25TBG (Note 35)	2.5 V	V			
NCP715MX30TBG (Note 35)	3.0 V	Y			
NCP715MX33TBG (Note 35)	3.3 V	2			
NCP715MX50TBG (Note 35)	5.0 V	5			
NCP715MX53TBG (Note 35)	5.3 V	5	+180°		
NCP715SN12T1G	1.2 V	PZD	–	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP715SN15T1G	1.5 V	PZE	–		
NCP715SN18T1G	1.8 V	PZF	–		
NCP715SN25T1G	2.5 V	PZG	–		
NCP715SN30T1G	3.0 V	PZH	–		
NCP715SN33T1G	3.3 V	PZJ	–		
NCP715SN50T1G	5.0 V	PZK	–		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

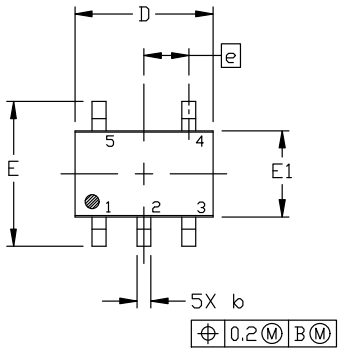
35. Products processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.

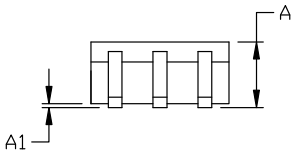
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

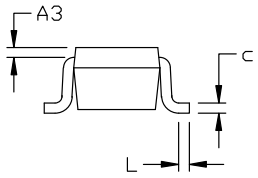
SCALE 2:1

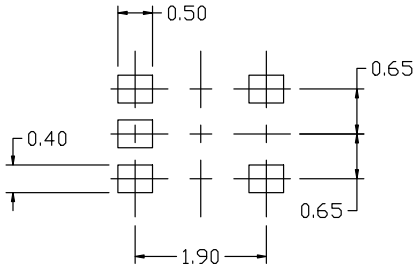
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

DATE 11 APR 2023









RECOMMENDED
MOUNTING FOOTPRINT

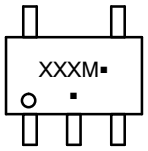
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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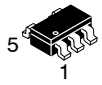
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

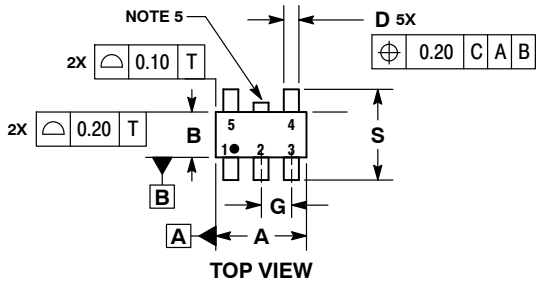
ON Semiconductor®



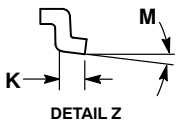
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

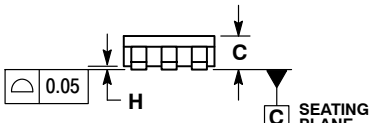
DATE 12 AUG 2020



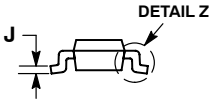
TOP VIEW



DETAIL Z



SIDE VIEW

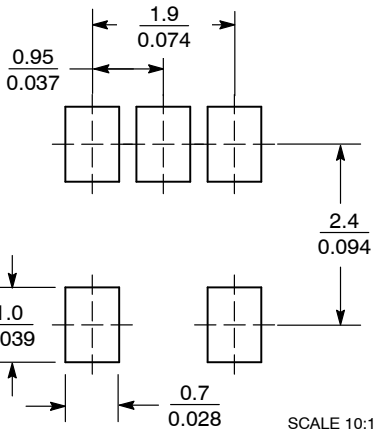


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

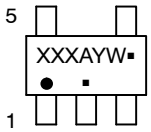
SOLDERING FOOTPRINT*



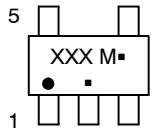
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSOP−5	PAGE 1 OF 1

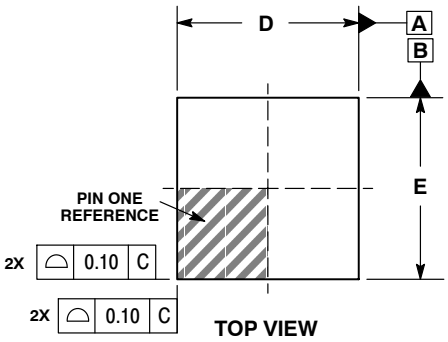
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

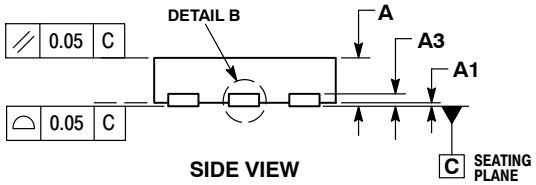
XDFN6 1.5x1.5, 0.5P
CASE 711AE
ISSUE B

SCALE 4:1

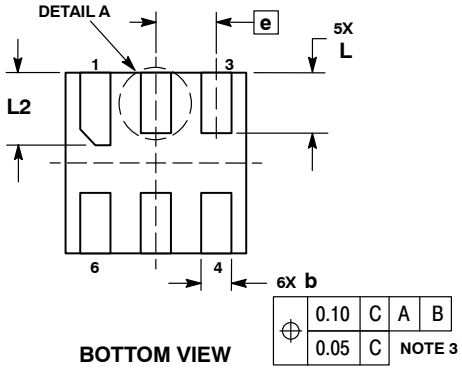
DATE 27 AUG 2015



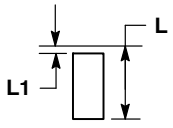
TOP VIEW



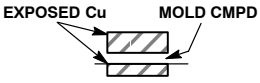
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

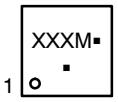


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.35	0.45
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.50 BSC	
E	1.50 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

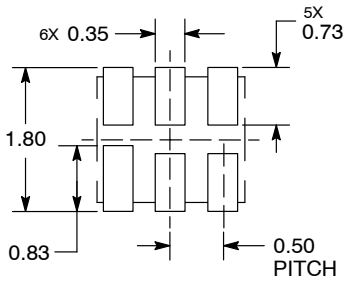
GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**XDFN6, 1.5 X 1.5, 0.5 P**	**PAGE 1 OF 1**

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