

# NCP4543

## ecoSwitch™ Advanced Load Management Controlled Load Switch with Low R<sub>ON</sub>

The NCP4543 load switch provides a component and area-reducing solution for efficient power domain switching with inrush current limit via soft start. It is designed to integrate control and driver functionality with a high performance low on-resistance power MOSFET in a single device. This cost effective solution is ideal for power management and hot-swap applications requiring low power consumption in a small footprint.

### Features

- Advanced Controller with Charge Pump
- Integrated N-Channel MOSFET with ESD Protection
- Soft-Start via Adjustable Slew Rate Control
- Low On-Resistance
- Input Voltage Range 0.5 V to 6 V
- Low Standby Current
- Load Bleed Function
- No External Components Required
- Enable Pins with CMOS Input Levels
- This is a Pb-Free Device

### Typical Applications

- Notebook and Tablet Computers
- Handheld Electronics
- Digital Cameras
- Portable Medical Devices
- Hard Drives
- Peripheral Ports

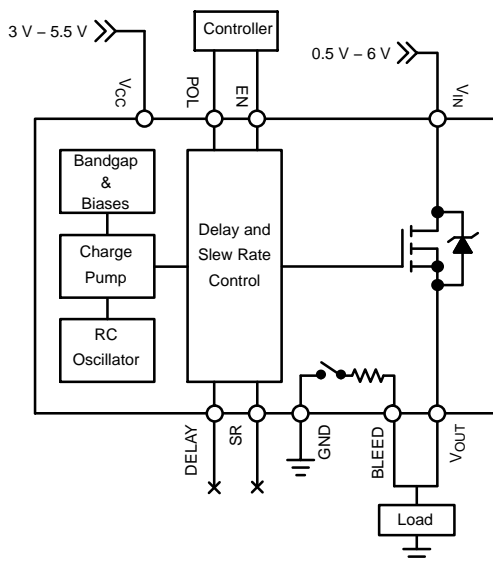


Figure 1. Typical Application – No external components included



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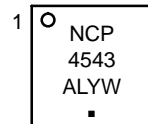
[www.onsemi.com](http://www.onsemi.com)

R <sub>ON</sub> TYP	V <sub>CC</sub>	V <sub>IN</sub>	I <sub>MAX</sub>
10.2 mΩ	5.0 V	1.8 V	7.3 A
12.2 mΩ	3.3 V	5.0 V	



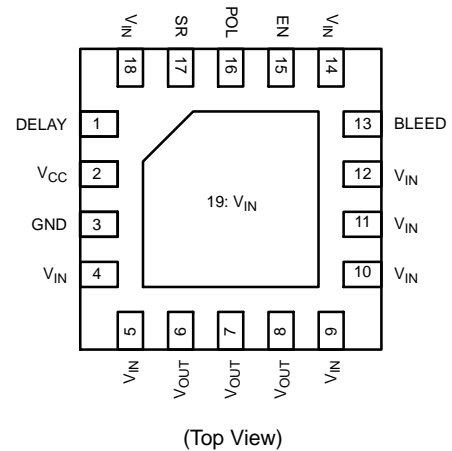
QFN18, 3x3  
CASE 485BF

### MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

### PIN CONFIGURATION



### ORDERING INFORMATION

Device	Package	Shipping†
NCP4543IMN5RG-A	QFN18 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP4543

## PIN DESCRIPTION

Pin	Name	Function															
1	DELAY	Turn-on delay adjustment															
2	V <sub>CC</sub>	Supply voltage to controller (3.0 V – 5.5 V)															
3	GND	Controller ground															
4, 5, 9–12, 14, 18, 19	V <sub>IN</sub>	Drain of MOSFET (0.5 V – 6.0 V)															
6–8	V <sub>OUT</sub>	Source of MOSFET connected to load															
13	BLEED	Load bleed connection															
15	EN	Digital input used to turn on the MOSFET according to this truth table: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>EN</th> <th>POL</th> <th>MOSFET</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>On</td> </tr> <tr> <td>0</td> <td>1</td> <td>Off</td> </tr> <tr> <td>1</td> <td>0</td> <td>Off</td> </tr> <tr> <td>1</td> <td>1</td> <td>On</td> </tr> </tbody> </table>	EN	POL	MOSFET	0	0	On	0	1	Off	1	0	Off	1	1	On
EN	POL	MOSFET															
0	0	On															
0	1	Off															
1	0	Off															
1	1	On															
16	POL	EN has an internal pull down resistor to GND POL has an internal pull up resistor to V <sub>CC</sub>															
17	SR	Slew rate adjustment															

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V <sub>CC</sub>	–0.3 to 6	V
Input Voltage Range	V <sub>IN</sub>	–0.3 to 6	V
Output Voltage Range	V <sub>OUT</sub>	–0.3 to 6	V
EN/POL Digital Input Range	V <sub>EN</sub>	–0.3 to (V <sub>CC</sub> + 0.3)	V
Thermal Resistance, Junction-to-Air (Note 1)	R <sub>θJA</sub>	49.5	°C/W
Thermal Resistance, Junction-to-Air (Note 2)	R <sub>θJA</sub>	32.9	°C/W
Thermal Resistance, Junction-to-Case (V <sub>IN</sub> Paddle)	R <sub>θJC</sub>	3.6	°C/W
Continuous MOSFET Current (Note 3)	I <sub>MAX</sub>	7.3	A
Total Power Dissipation @ T <sub>A</sub> = 25°C (Notes 1 and 4) Derate above T <sub>A</sub> = 25°C	P <sub>D</sub>	1.31 20.2	W mW/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C (Notes 2 and 4) Derate above T <sub>A</sub> = 25°C	P <sub>D</sub>	1.98 30.4	W mW/°C
Storage Temperature Range	T <sub>STG</sub>	–40 to 150	°C
Lead Temperature, Soldering (10 sec.)	T <sub>SLD</sub>	260	°C
ESD Capability, Human Body Model (Note 5)	ESD <sub>HBM</sub>	3.5	kV
ESD Capability, Machine Model (Note 5)	ESD <sub>MM</sub>	200	V
ESD Capability, Charged Device Model (Note 5)	ESD <sub>CDM</sub>	1	kV
Latch-up Current Immunity (Note 5)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Surface-mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.
- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Current limited by package.
- Specified for derating purposes only, ensure that I<sub>MAX</sub> is never exceeded.
- Tested by the following methods @ T<sub>A</sub> = 25°C:  
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD Machine Model tested per EIA/JESD22-A115  
 ESD Charged Device Model per ESD-STM5.3.1-1999  
 Latch-up Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78

# NCP4543

## RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage	$V_{CC}$	3	5.5	V
Input Voltage	$V_{IN}$	0.5	6	V
Ground	GND		0	V
Ambient Temperature	$T_A$	0	70	°C
Junction Temperature	$T_J$	0	90	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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### MOSFET

On-Resistance	$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$	$R_{ON}$		10.2	13	m $\Omega$
	$V_{CC} = 5.0\text{ V}; V_{IN} = 5.0\text{ V}$			10.5	13.5	
	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$			11	14	
	$V_{CC} = 3.3\text{ V}; V_{IN} = 5.0\text{ V}$			12.2	16	
Leakage Current (Note 6)	$V_{EN} = 0\text{ V}; V_{POL} = V_{CC}; V_{IN} = 6\text{ V}$	$I_{LEAK}$		0.02	1.0	$\mu\text{A}$

### CONTROLLER

Supply Standby Current (Note 7)	$V_{EN} = 0\text{ V}; V_{POL} = V_{CC} = 5.5\text{ V}$	$I_{STBY}$		5.0	15	$\mu\text{A}$
Supply Dynamic Current (Note 8)	$V_{EN} = V_{POL} = V_{CC}$	$I_{DYN}$		250	500	$\mu\text{A}$
Bleed Resistance		$R_{BLEED}$	50	100	200	$\Omega$
Input High Voltage – EN & POL		$V_{IH}$	2.0			V
Input Low Voltage – EN & POL		$V_{IL}$			0.8	V
Pull Down Resistance – EN		$R_{PD}$	40	100	180	k $\Omega$
Pull Up Resistance – POL		$R_{PU}$	40	100	180	k $\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Average current from  $V_{IN}$  to  $V_{OUT}$  with MOSFET turned off.

7. Average current from  $V_{CC}$  to GND with MOSFET turned off.

8. Average current from  $V_{CC}$  to GND after charge up time of MOSFET.

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## SWITCHING CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified, Note 9)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
$V_{CC} = 5.0\text{ V}$ , $V_{IN} = 1.8\text{ V}$						
Output Slew Rate	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	SR		8.1		kV/s
Output Turn-on Delay	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	$T_{ON}$		540		$\mu\text{s}$
Output Turn-off Delay	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	$T_{OFF}$		1.2		$\mu\text{s}$
$V_{CC} = 3.3\text{ V}$ , $V_{IN} = 5.0\text{ V}$						
Output Slew Rate	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	SR		8.5		kV/s
Output Turn-on Delay	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	$T_{ON}$		670		$\mu\text{s}$
Output Turn-off Delay	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	$T_{OFF}$		0.8		$\mu\text{s}$

9. See below figure for Test Circuit and Timing Diagrams.

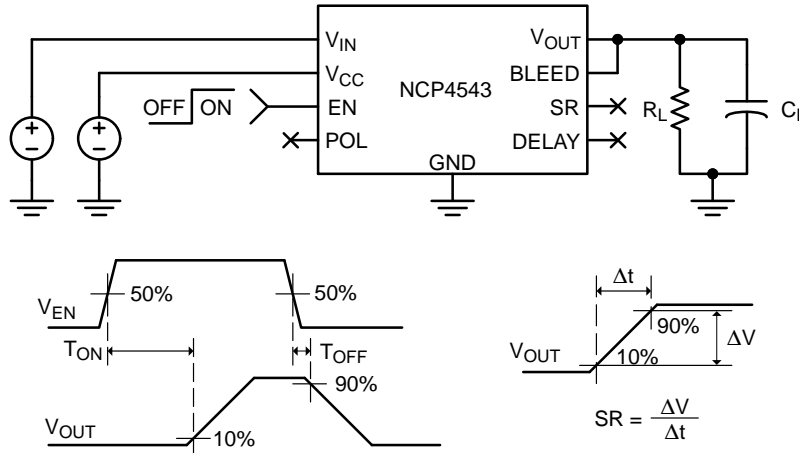


Figure 2. Test Circuit and Timing Diagrams

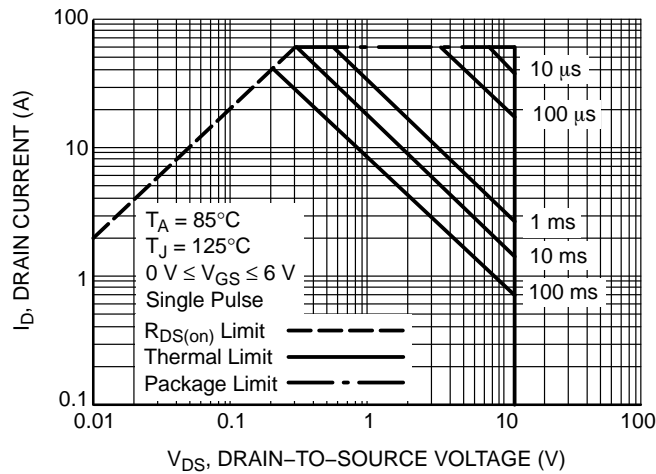


Figure 3. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

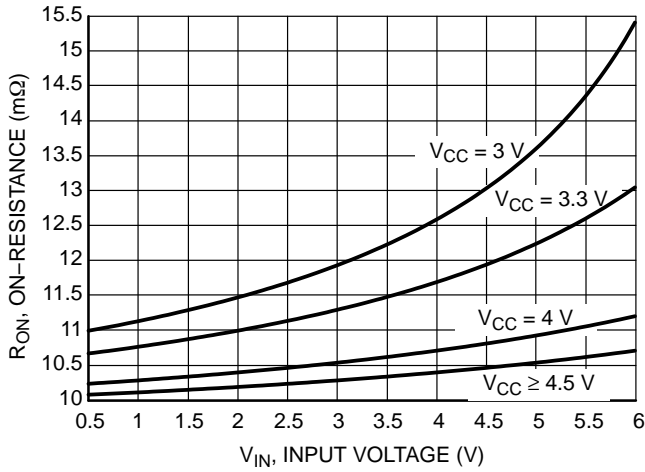


Figure 4. On-Resistance vs. Input Voltage

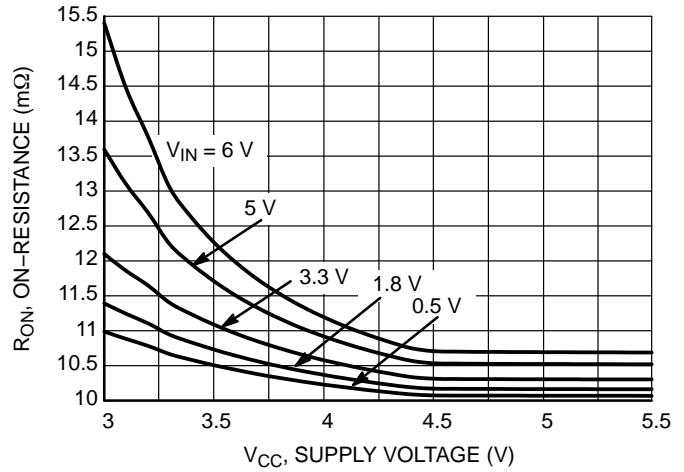


Figure 5. On-Resistance vs. Supply Voltage

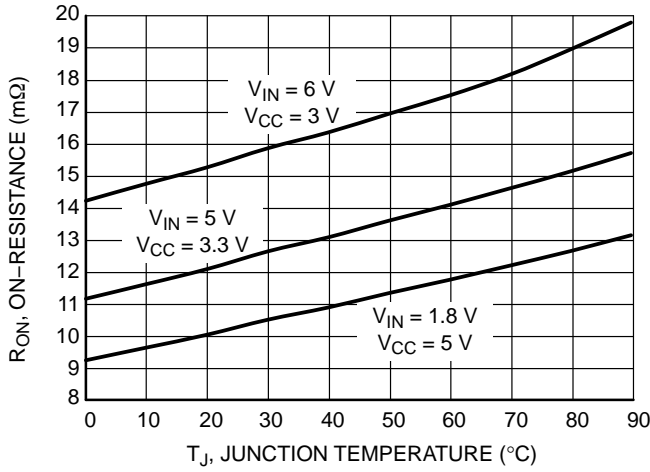


Figure 6. On-Resistance vs. Temperature

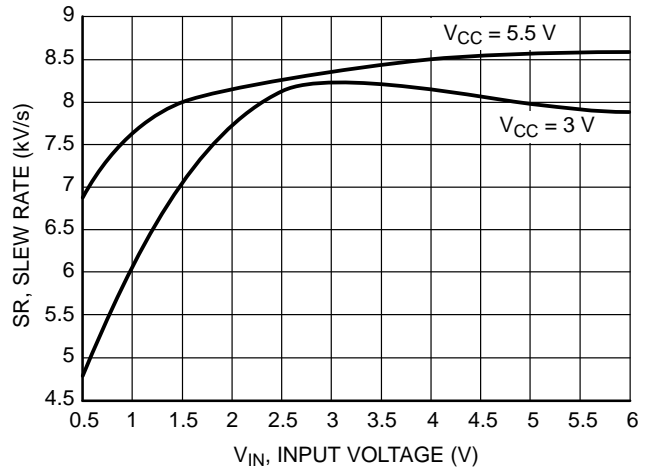


Figure 7. Slew Rate vs. Input Voltage

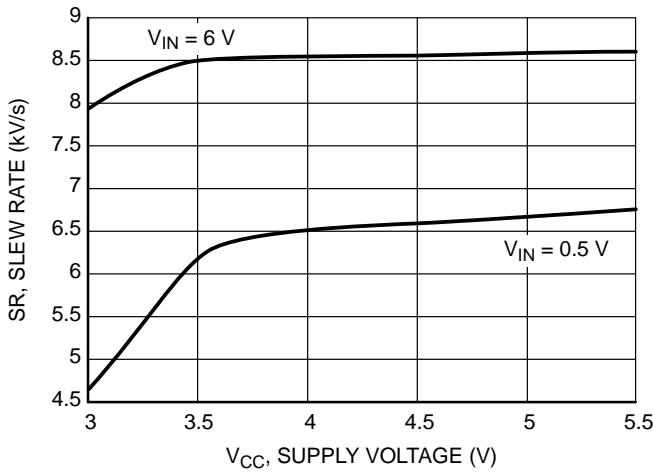


Figure 8. Slew Rate vs. Supply Voltage

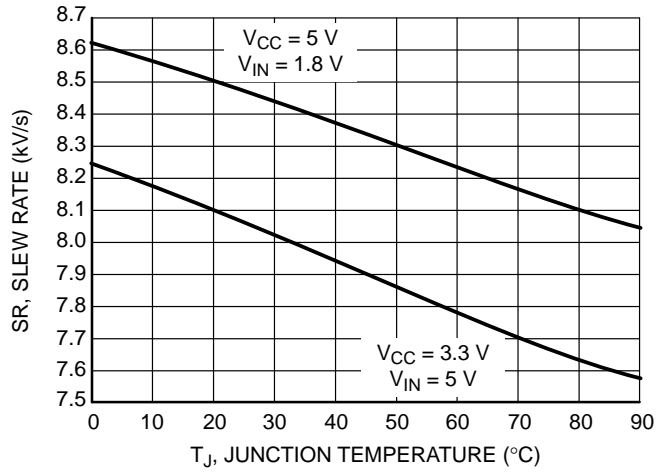


Figure 9. Slew Rate vs. Temperature

TYPICAL CHARACTERISTICS

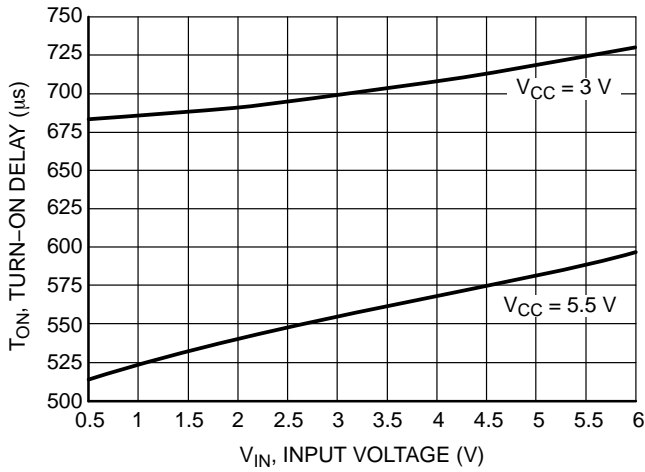


Figure 10. Turn-On Delay vs. Input Voltage

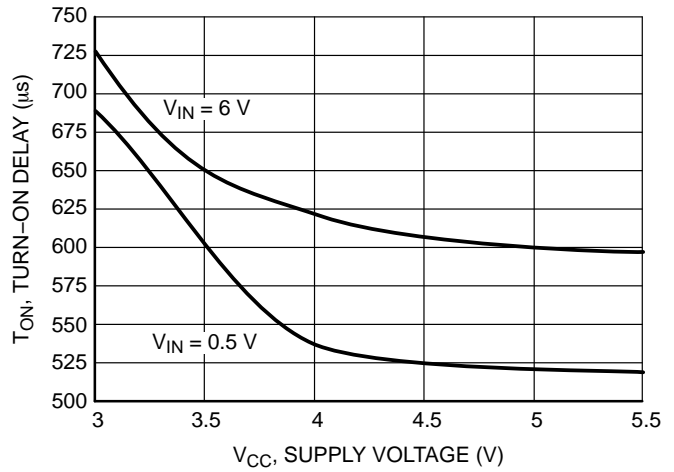


Figure 11. Turn-On Delay vs. Supply Voltage

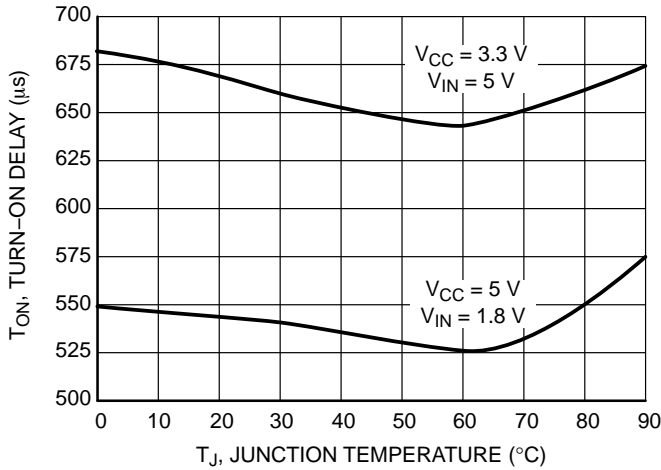


Figure 12. Turn-On Delay vs. Temperature

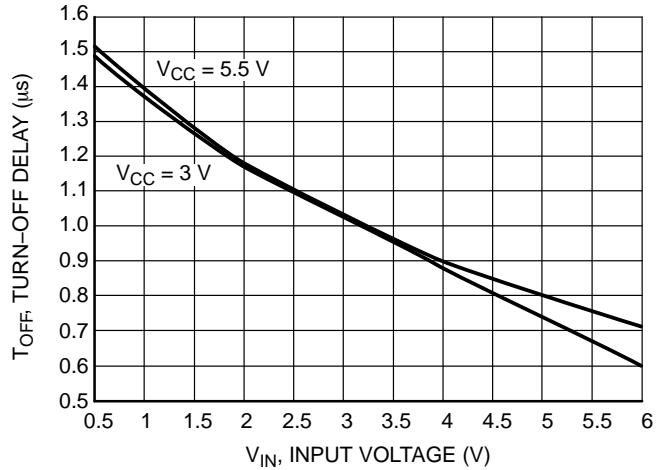


Figure 13. Turn-Off Delay vs. Input Voltage

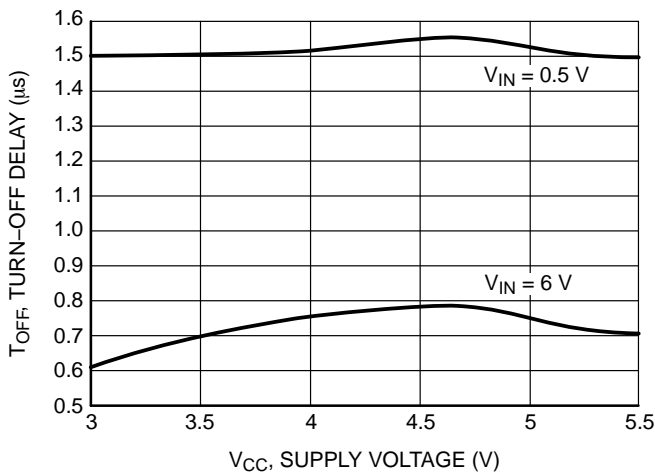


Figure 14. Turn-Off Delay vs. Supply Voltage

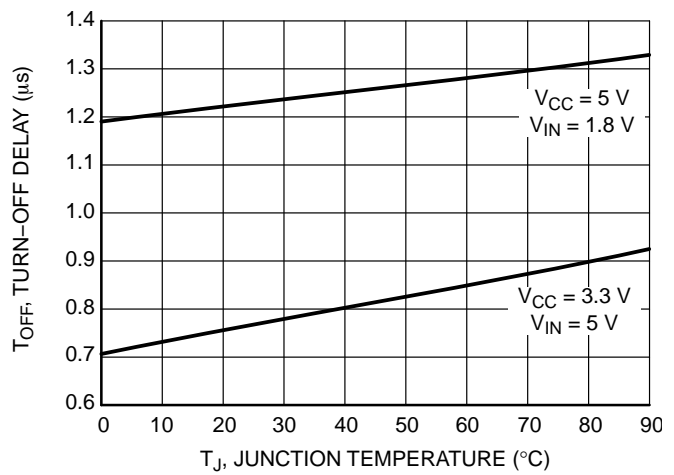


Figure 15. Turn-Off Delay vs. Temperature

# NCP4543

## TYPICAL CHARACTERISTICS

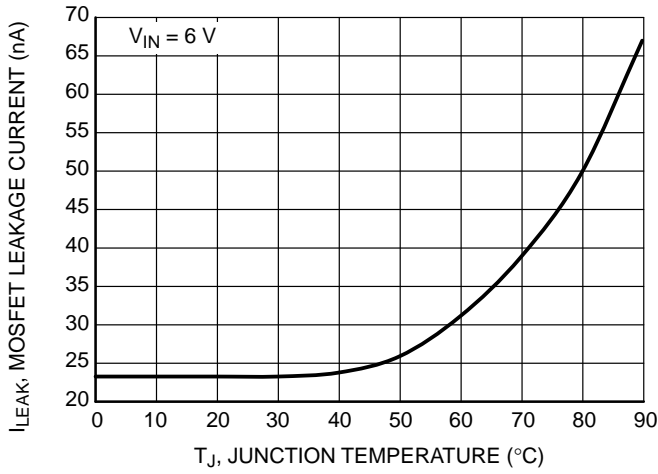


Figure 16. MOSFET Leakage Current vs. Temperature

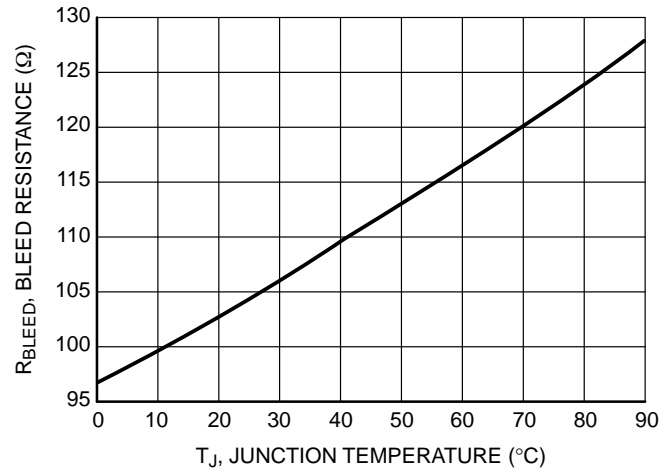


Figure 17. Bleed Resistance vs. Temperature

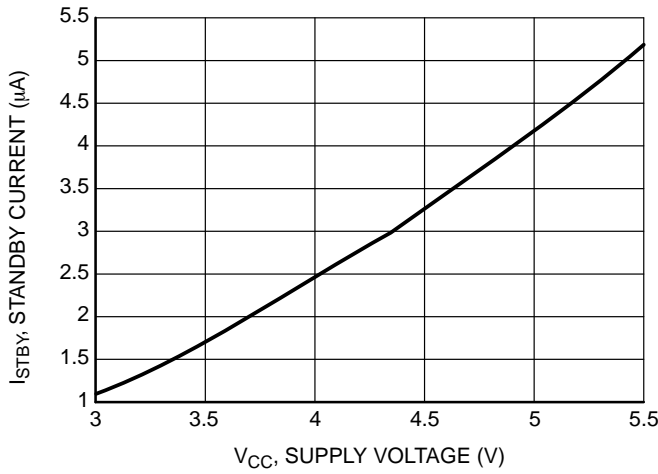


Figure 18. Standby Current vs. Supply Voltage

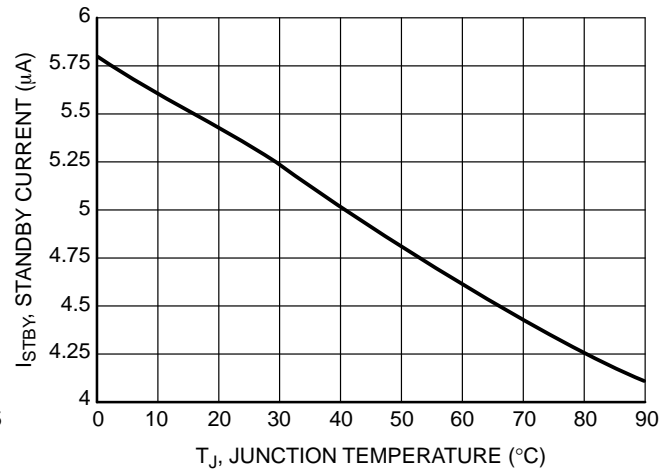


Figure 19. Standby Current vs. Temperature

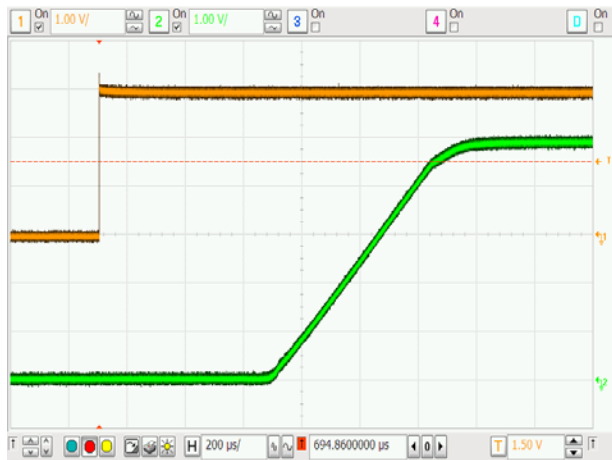


Figure 20. Turn-on Response  
(V<sub>CC</sub> = 3.3 V, V<sub>IN</sub> = 5.0 V, R<sub>L</sub> = 10 Ω, C<sub>L</sub> = 0.1 μF)

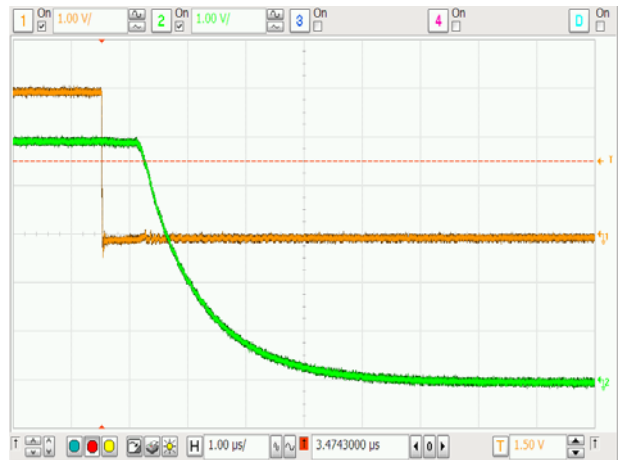


Figure 21. Turn-off Response  
(V<sub>CC</sub> = 3.3 V, V<sub>IN</sub> = 5.0 V, R<sub>L</sub> = 10 Ω, C<sub>L</sub> = 0.1 μF)

## APPLICATIONS INFORMATION

**On-Resistance**

The MOSFET gate voltage in the NCP4543 is driven by a charge pump in the controller circuit. The output voltage of the charge pump is dependent on the voltage on  $V_{CC}$ . The  $R_{ON}$  of the MOSFET is in turn dependent on its  $V_{GS}$ . Care must be taken to ensure a sufficient  $V_{CC}$  voltage is used to create the desired  $R_{ON}$  given the anticipated input voltage.

**Enable Control**

The NCP4543 allows for enabling the MOSFET in either an active-high or active-low configuration. When the EN and POL pins are both at a logic high level or both at a logic low level and the  $V_{CC}$  supply pin has an adequate voltage applied, the MOSFET will be enabled. Similarly, when the EN and POL pins are at different logic levels, the MOSFET will be disabled.

An internal pull down resistor on the EN pin and an internal pull up resistor on the POL pin ensure that the MOSFET will be disabled when neither pin is driven. The internal pull down or pull up resistor can also be used to allow for only one of the pins to be driven in either an active-high or active-low state.

**Parametric Adjustments**

The NCP4543 can be used in several configurations depending on the need to control turn-on delay, slew rate, and bleed resistance. Default minimum values of each parameter are built into the part without the requirement of external components. This configuration is shown above in Figure 1.

Figures 22 and 23 show alternate configurations where external components are used to modify the turn-on delay, slew rate, and total bleed resistance.

Figure 22 shows an external capacitor,  $C_{COMBO}$ , connected from the  $V_{OUT}$  pin to both the DELAY and SR pins. This allows for one external capacitor to be used to modify the turn-on delay and slew rate. Note that the value of  $C_{COMBO}$  is used in Equations 1 and 2 (below) in place of  $C_{DEL}$  and  $C_{SR}$  respectively.

Figure 23 shows the use of two external capacitors for independent control of the turn-on delay and slew rate.

**Turn-On Delay**

The NCP4543 provides a time delay between the input transitions on EN (or POL) to the MOSFET turning on. The

turn-on delay can be increased with an external capacitor added between the DELAY pin and either ground or the  $V_{OUT}$  pin as shown in Figures 22 and 23.

The total delay is calculated by adding the default turn-on delay to a delta term which is calculated as follows:

$$\Delta t = K_{DEL} * C_{DEL} \quad (\text{eq. 1})$$

where  $K_{DEL}$  is a constant and  $C_{DEL}$  is the off-chip capacitance added between the DELAY pin to either ground or the  $V_{OUT}$  pin (see table below). When no external capacitor is present, the delay will be the specified default turn-on delay.

**Slew Rate Control**

The NCP4543 is equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables this device to be used in hot swapping applications. The slew rate can be decreased with an external capacitor added between the SR pin and the  $V_{OUT}$  pin as shown in Figures 22 and 23.

The slew rate can be calculated as follows:

$$SR = \frac{K_{SR}}{C_{SR} + C_{CHIP}} \quad (\text{eq. 2})$$

where  $K_{SR}$  is a constant,  $C_{SR}$  is the off-chip capacitance added between the SR pin and the  $V_{OUT}$  pin, and  $C_{CHIP}$  is the on-chip capacitance (see table below). Note that this equation is only valid for  $C_{SR} \geq 470$  pF. When no external capacitor is present, the slew rate will be the specified default slew rate.

**Load Bleed**

The NCP4543 has an on-chip bleed resistor that can be used to bleed the charge off of the load to ground after the MOSFET has been disabled. In series with the bleed resistor is a bleed switch which is enabled whenever the MOSFET is disabled. Delays are added to the enable of this switch to ensure that both the MOSFET and the bleed switch are not concurrently active. The total bleed resistance can be increased by adding a resistor between the BLEED pin and the  $V_{OUT}$  pin as shown in Figures 22 and 23. If the load bleed function is not desired, the BLEED pin should be tied to ground or left floating.

**SLEW RATE AND TURN-ON DELAY**

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Turn-on Delay Constant		$K_{DEL}$		1.74		M $\Omega$
External Delay Capacitance (Note 10)	Between DEL pin and GND	$C_{DEL}$			10	nF
Slew Rate Constant		$K_{SR}$		1.4		$\mu$ A
External Slew Rate Capacitance (Note 10)	Between SR pin and $V_{OUT}$ pin	$C_{SR}$			2	nF
Internal Slew Rate Capacitance		$C_{CHIP}$		150		pF
External Combo Capacitance (Note 10)	Between SR & DEL pins and $V_{OUT}$ pin	$C_{COMBO}$			2	nF

10. Recommended range, larger values may be used but may degrade the performance of the part



# NCP4543

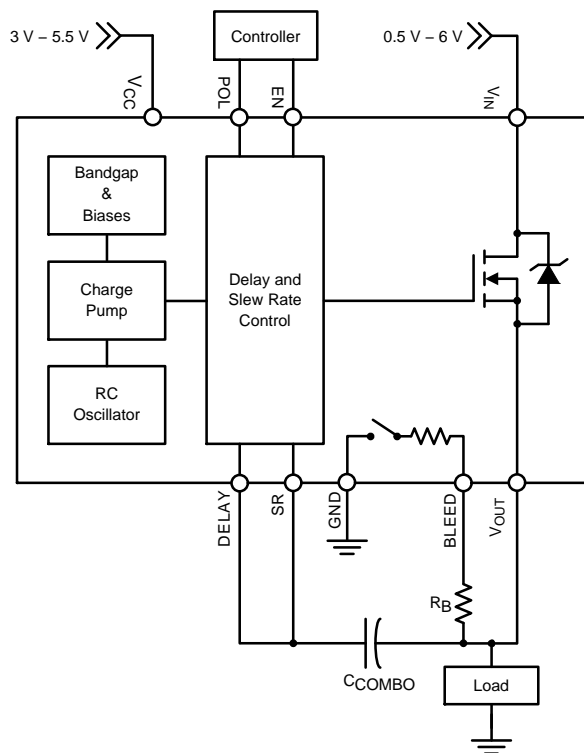


Figure 22. Example Application – External bleed resistor with single-capacitor adjustment of turn-on delay and slew rate.

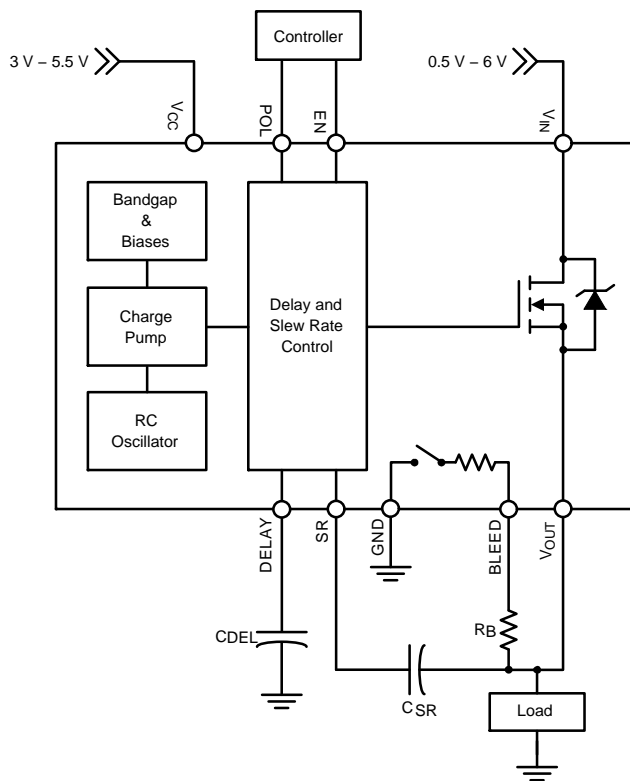


Figure 23. Example Application – External bleed resistor with independent adjustment of turn-on delay and slew rate.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

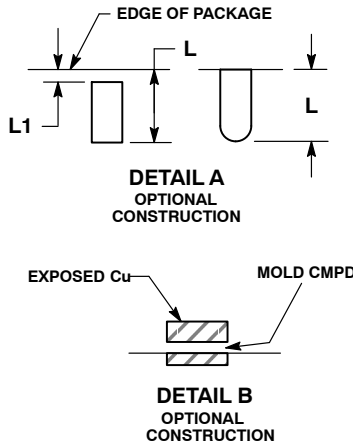
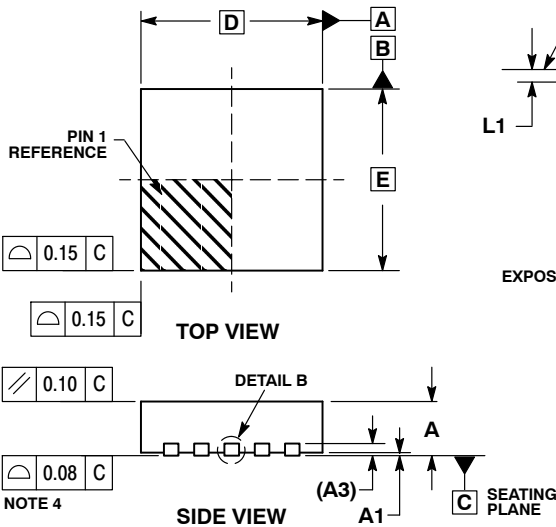
ON Semiconductor®



SCALE 2:1

**QFN18 3x3, 0.5P**  
CASE 485BF-01  
ISSUE O

DATE 10 FEB 2010

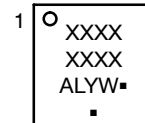


**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.75	1.95
E	3.00	BSC
E2	1.75	1.95
e	0.50	BSC
K	0.20	---
L	0.275	0.375
L1	0.00	0.15

**GENERIC MARKING DIAGRAM\***

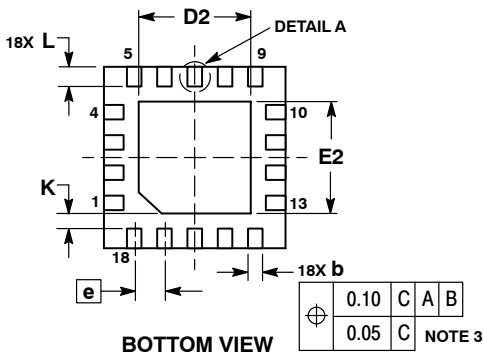


- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

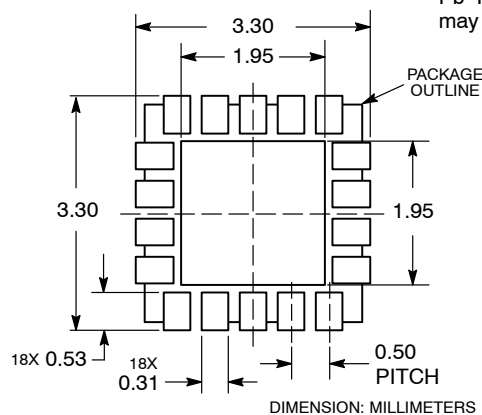
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "▪", may or may not be present.



**RECOMMENDED MOUNTING FOOTPRINT**



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON48573E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>QFN18 3X3, 0.5P</b>	<b>PAGE 1 OF 1</b>

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