NCP432, NCP433

1.5A Ultra-Small Controlled Load Switch with Auto-Discharge Path

The NCP432 and NCP433 are a low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC's on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output (NCP433 only).

Proposed in wide input voltage range from 1.0 V to 3.6 V, and a very small 0.76 x 0.76 mm WLCSP4, 0.4 mm pitch.

Features

- 1 V – 3.6 V Operating Range
- 50 mΩ P MOSFET at 1.8 V
- DC Current up to 1.5 A
- Output Auto−discharge (NCP433)
- Active High EN Pin
- WLCSP4 0.76 x 0.76 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

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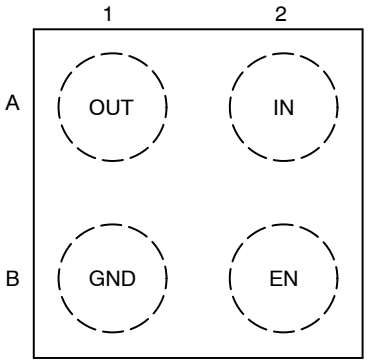
MARKING DIAGRAM

WLCSP4
CASE 567FJ

XX

XX = AV or AT

PINOUT



(Top View)

ORDERING AND MARKING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

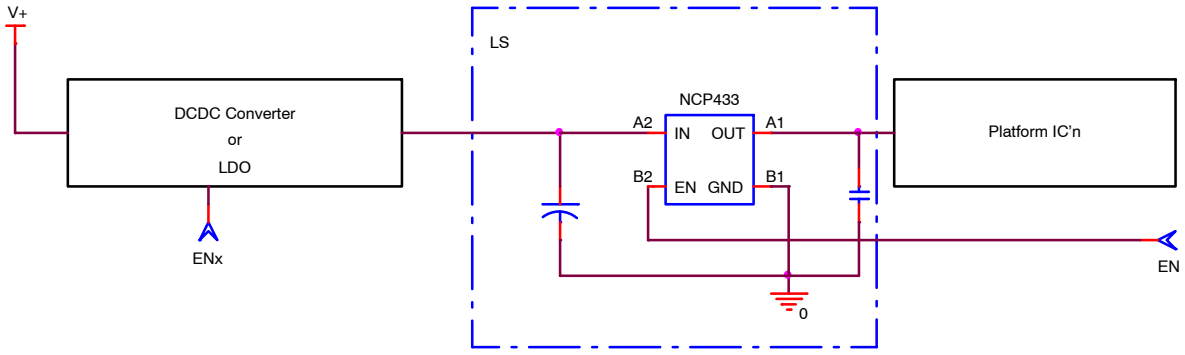


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2	POWER	Load−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	B1	POWER	Ground connection.
EN	B2	INPUT	Enable input, logic high turns on power switch.
OUT	A1	OUTPUT	Load−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

BLOCK DIAGRAM

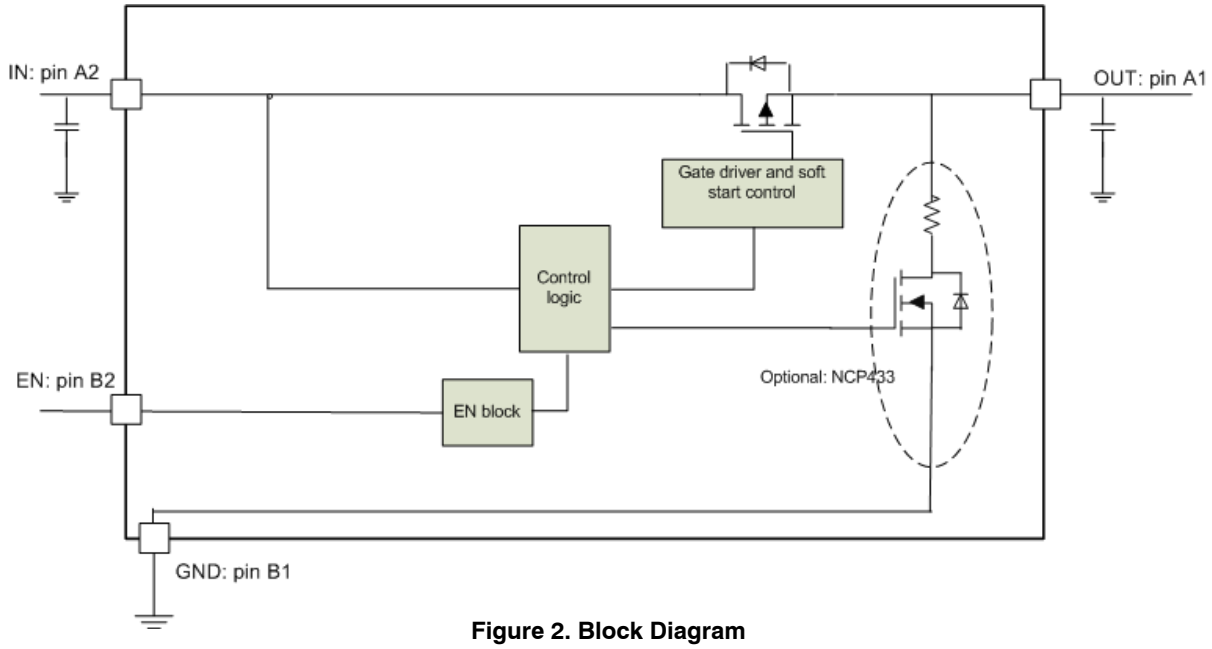


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins:	V_{EN}, V_{IN}, V_{OUT}	−0.3 to + 4.0	V
From IN to OUT Pins: Input/Output	V_{IN}, V_{OUT}	0 to + 4.0	V
Maximum Junction Temperature	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Human Body Model (HBM) ESD Rating are (Notes 1 and 2)	ESD HBM	7000	V
Machine Model (MM) ESD Rating are (Notes 1 and 2)	ESD MM	250	V
Charge Device Model (CDM) ESD Rating are (Notes 1 and 2)	ESD CDM	2000	V
Latch−up protection (Note 3) − Pins IN, OUT, EN	LU	 100	mA
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±7.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±250 V per JEDEC standard: JESD22−A115 for all pins.
   Charge Device Model (CDM) ±2.0 kV per JEDEC standard: JESD22−C101 for all pins.
3. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.0		3.6	V
V_{EN}	Enable Voltage			0		3.6	
T_A	Ambient Temperature Range			−40	25	+85	°C
C_{IN}	Decoupling input capacitor			1			μF
C_{OUT}	Decoupling output capacitor			1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 5)			150		°C/W
I_{OUT}	Maximum DC current					1.5	A
P_D	Power Dissipation Rating (Note 6)	$T_A \le 25°C$	WLCSP package		0.5		W
		$T_A = 85°C$	WLCSP package		0.2		W

5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation (P_D) is given by the following formula:

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.0 V to 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and V_{IN} = 3.3 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance	V_{IN} = 3.6 V	T_A = 25 °C, I = 200 mA (Note 8)		35		mΩ
			T_A = 85°C			55	
		V_{IN} = 3.3 V	T_A = 25°C, I = 200 mA		37		
			T_A = 85°C			60	
		V_{IN} = 1.8 V	T_A = 25°C, I = 200 mA		50		
			T_A = 85°C			80	
		V_{IN} = 1.2 V	T_A = 25°C, I = 200 mA		100		
			T_A = 85°C			150	
		V_{IN} = 1.1 V	T_A = 25°C, I = 100 mA		120		
R_{DIS}	Output discharge path	EN = low	V_{IN} = 3.3 V, NCP433 only	40	65	90	Ω
T_R	Output rise time	V_{IN} = 3.6 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω (Note 7) from 10% to 90% of V_{OUT}	5	20	40	μs
T_F	Output fall time		C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω (Note 7)	20	56	80	μs
T_{on}	Gate turn on		Gate turn on + Output rise time	20	47	115	μs
T_{en}	Enable time		From EN low to high to V_{OUT} 10%	15	30	75	μs
T_{dis}	Disable time		From EN high to low to V_{OUT} = 90% of fully on	2	11	20	μs
V_{IH}	High−level input voltage			0.9			V
V_{IL}	Low−level input voltage					0.5	V
QUIESCENT CURRENT							
I_Q	Current consumption	V_{IN} = 3.3 V, EN = low, No load			0.01	0.6	μA
		V_{IN} = 3.3 V, EN = high, No load			0.2	0.6	μA

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground
8. Guaranteed by design and characterization, not production tested.

TIMINGS

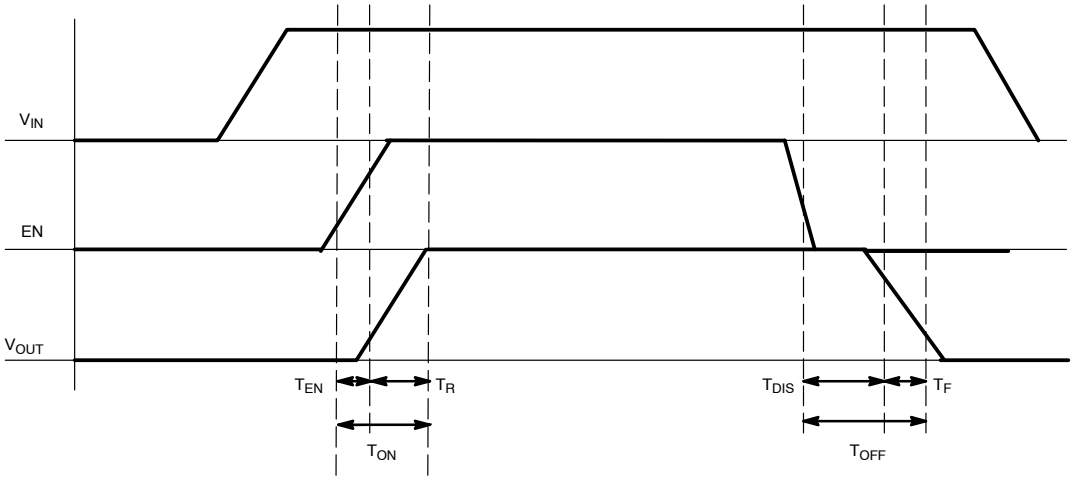


Figure 3. Enable, Rise and Fall Time

TYPICAL CHARACTERISTICS

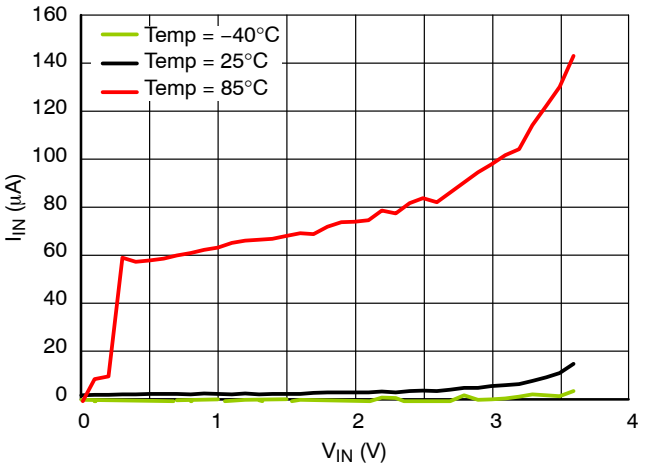


Figure 4. Standby Current versus Temperature

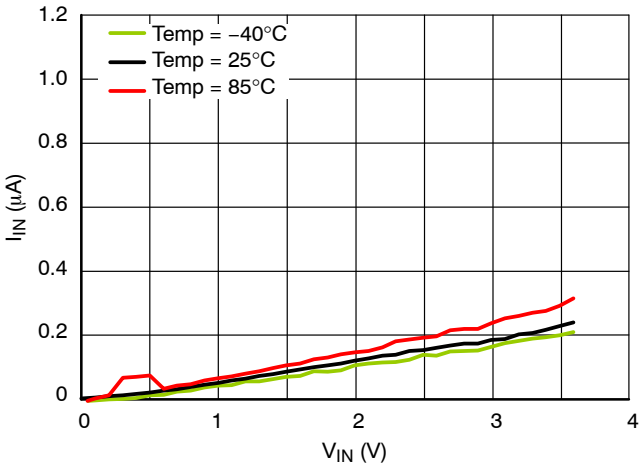


Figure 5. Quiescent Current versus Temperature

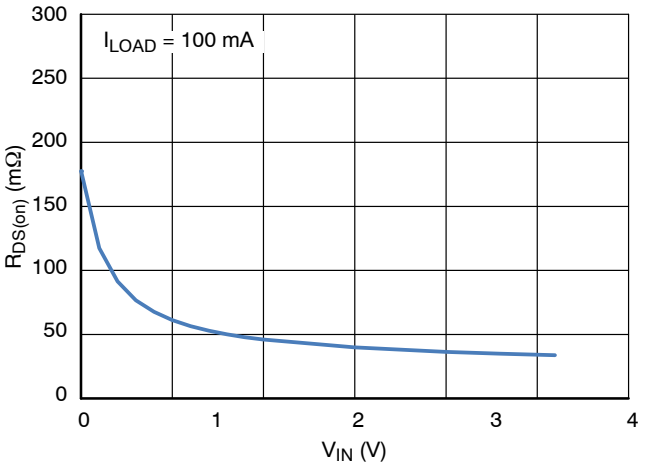


Figure 6. $R_{DS(on)}$ versus V_{IN}, 25°C, 100 mA Load

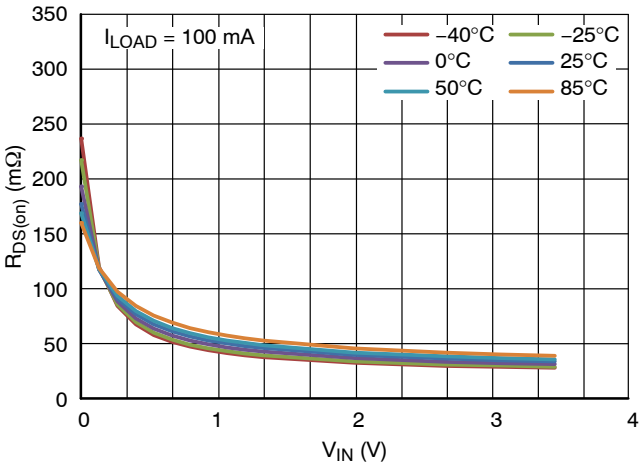


Figure 7. $R_{DS(on)}$ versus Temperature, 100 mA Load

FUNCTIONAL DESCRIPTION

Overview

The NCP432 – NCP433 are high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a range of battery from 1.0 V to 3.6 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of Vin of 1.0 V and EN forced to high level.

Auto Discharge (NCP433 only)

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_{IN} > 1.0 V.

In order to limit the current across the internal discharge N−MOSFET, the typical value is set at 65 Ω.

Cin and Cout Capacitors

IN and OUT, 1 μF, at least, capacitors must be placed as close as possible the part for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2$$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A$$

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

PCB Recommendations

The NCP432 – NCP433 integrate an up to 1.5 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

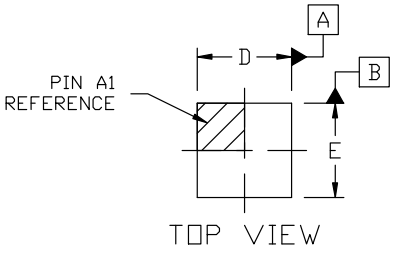
ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP432FCT2G	AV	WLCSP4 (Pb−Free)	3000 / Tape & Reel
NCP433FCT2G	AT	WLCSP4 (Pb−Free)	3000 / Tape & Reel

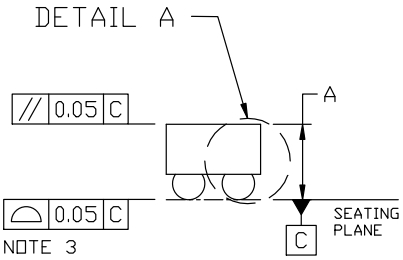
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WLCSP4 0.76x0.76x0.605
CASE 567FJ
ISSUE C

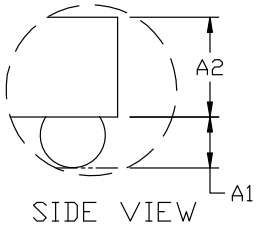
DATE 27 MAR 2023



TOP VIEW



SIDE VIEW

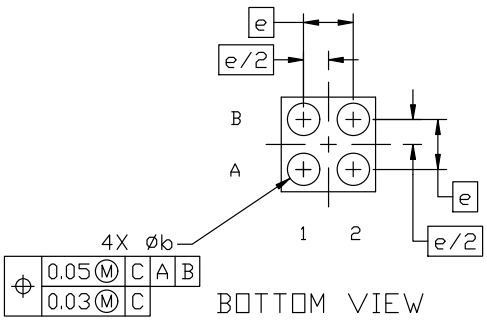


SIDE VIEW
SCALE 1:2

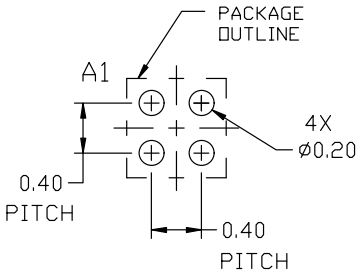
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.555	0.605	0.655
A1	0.180	0.205	0.230
A2	0.375	0.400	0.425
b	0.236	0.261	0.286
D	0.73	0.76	0.79
E	0.73	0.76	0.79
e	0.40 BSC		



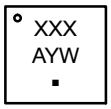
BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP4 0.76x0.76x0.605**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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