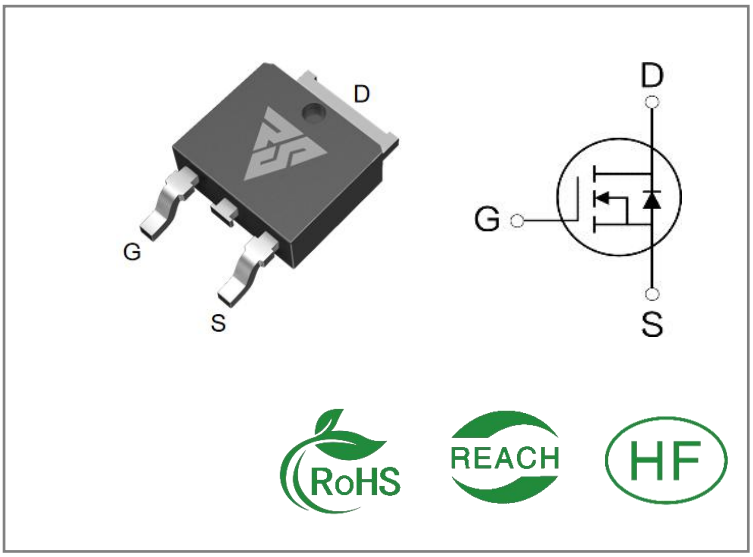
ID	R_{DS}(ON)(Typ)	VDSS
9A	0.68Ω	500V



Applications:
- Switch Mode Power Supply(SMPS)
- Adapter & Charger
- AC-DC Switching Power Supply

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS9N50D	T0-252	RS9N50D	Tape&reel	2500 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS9N50D	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current TC=25℃	9	A
IDM	Pulsed Drain Current (Note*1)	32	
PD	Power Dissipation	63	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L = 10mH, VDD = 50V, RG = 25Ω	180	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Copyright Reasunos

Thermal Resistance

Symbol	Parameter	RS9N50D	Units	Test Conditions
RθJC	Junction-to-Case	1.98	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500	--	--	V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=500V,VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	0.68	0.85	Ω	VGS=10V,ID=4A
VGS(TH)	Gate Threshold Voltage	3	--	4	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	32.5	--	nS	VDS=250V ID=4A RG=25Ω
trise	Rise Time	--	5.5	--		
td(OFF)	Turn- OFF Delay Time	--	74	--		
tfall	Fall Time	--	24	--		

Copyright Reasunos

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	940	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	104	--		
Crss	Reverse Transfer Capacitance	--	10	--		
Qg	Total Gate Charge	--	27.5	--	nC	VDS=400V ID=8A VGS=10V
Qgs	Gate- to- Source Charge	--	3.5	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	15	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	9	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	32	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=4A,VGS=0V
trr	Reverse Recovery Time	--	258	--	nS	VGS=0V IS=8A,di/dt=100A /μs
Qrr	Reverse Recovery Charge	--	2.6	--	μC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Copyright Reasunos

Typical Feature Curve

Figure 1. Output Characteristics (T_J = 25°C)

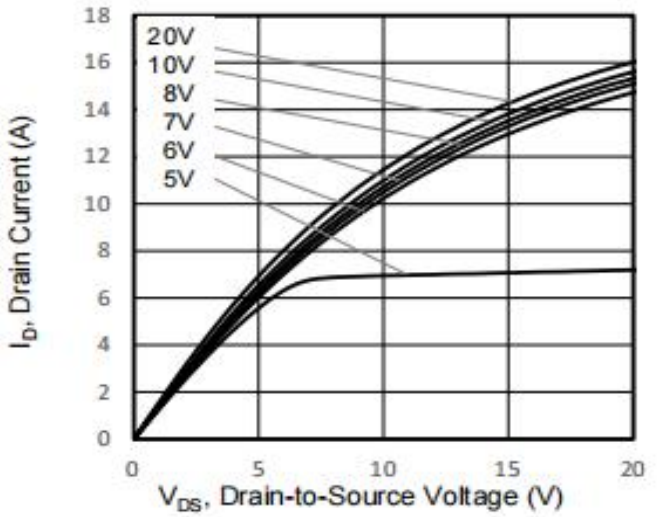


Figure 2. Body Diode Forward Voltage

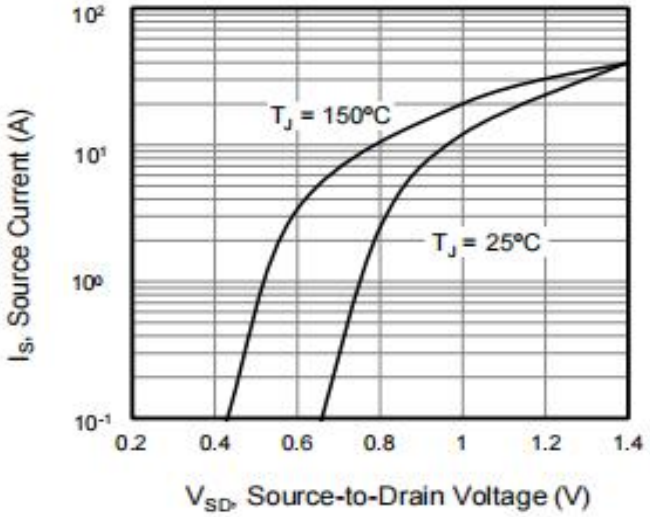


Figure 3. Drain Current vs. Temperature

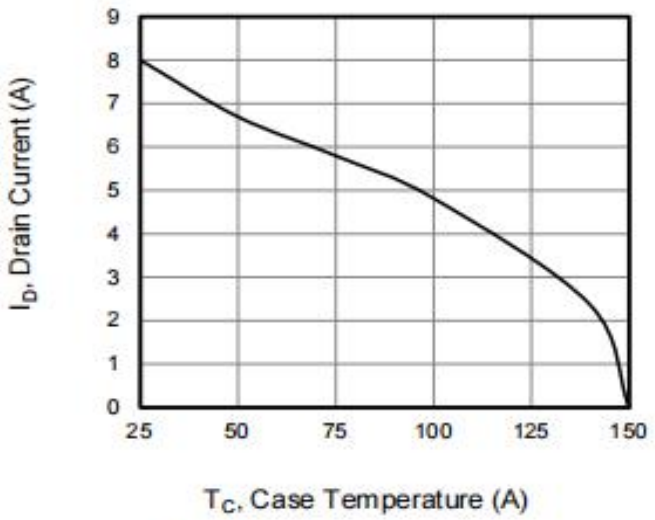


Figure 4. BV_{DSS} Variation vs. Temperature

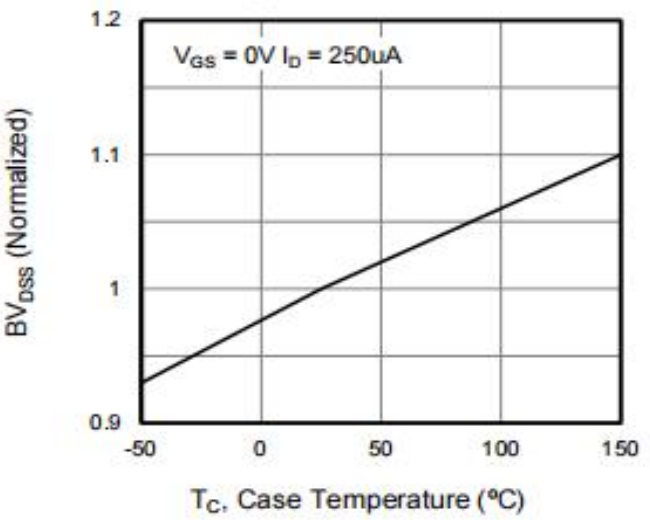


Figure 5. Transfer Characteristics

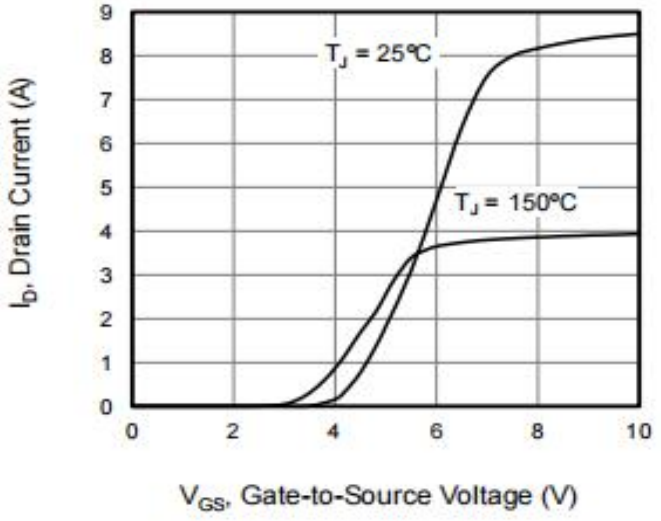
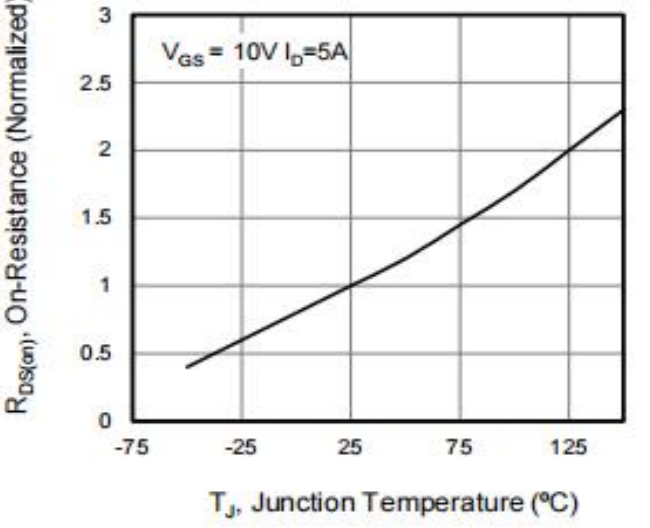


Figure 6. On-Resistance vs. Temperature



Copyright Reasunos

Figure 7. Capacitance

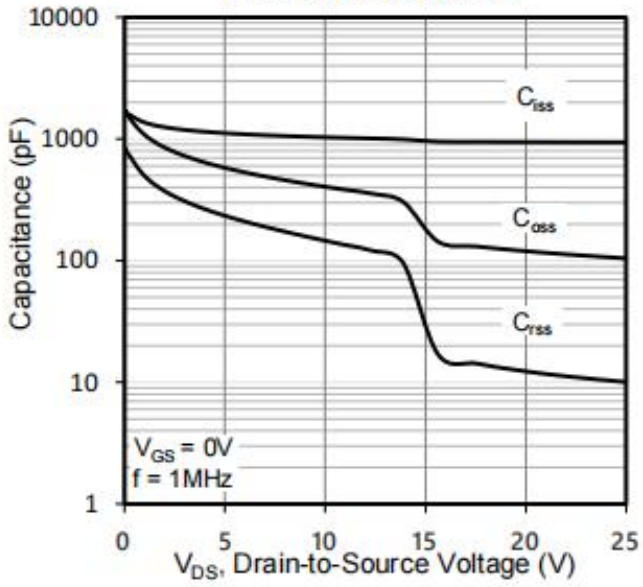


Figure 8. Gate Charge

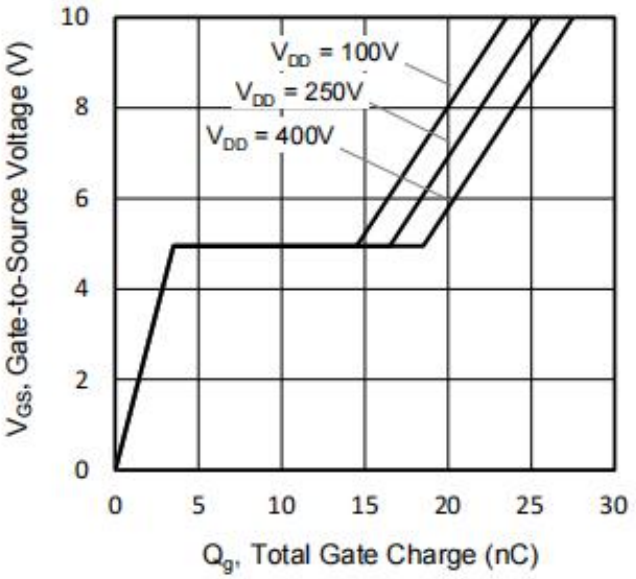
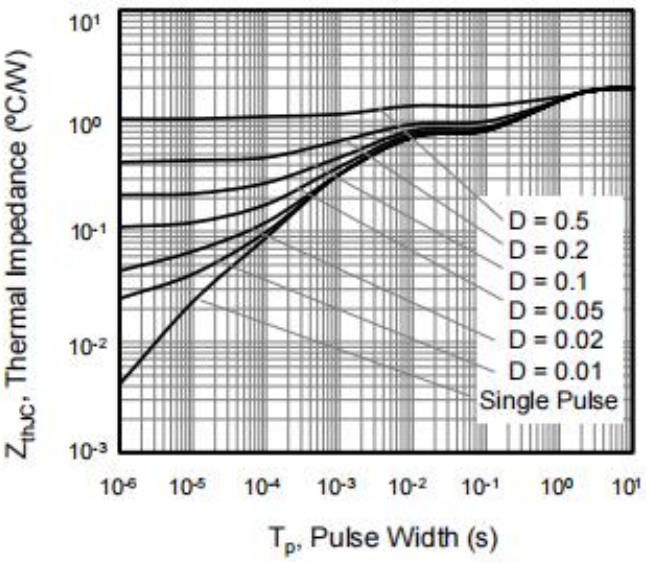


Figure 9. Transient Thermal Impedance



 Copyright Reasunos

Test Circuits and Waveforms

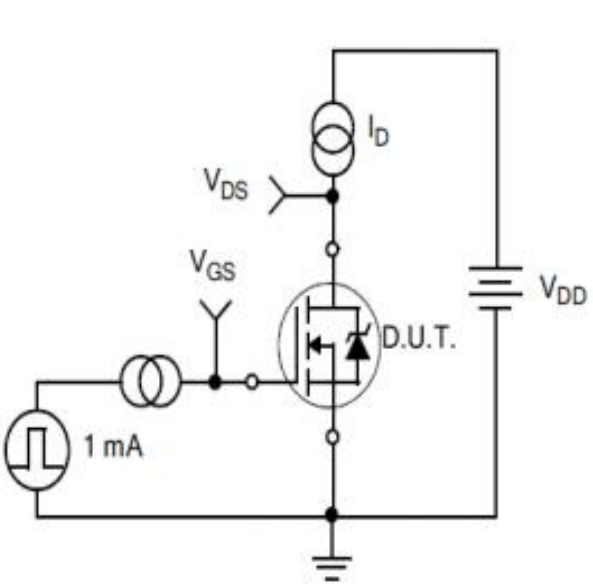


Figure10.
Gate Charge Test Circuit

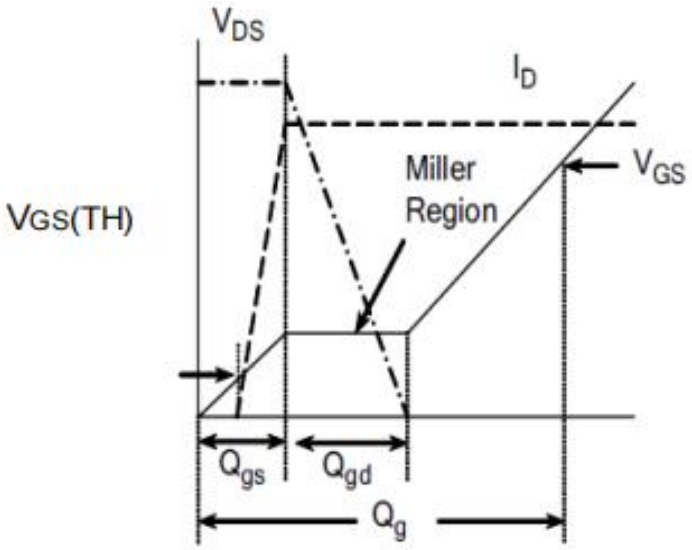


Figure11.
Gate Charge Waveform

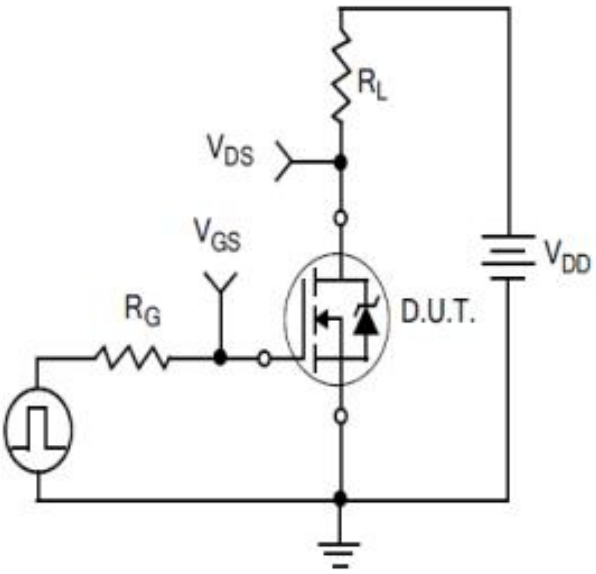


Figure12.
Resistive Switching Test Circuit

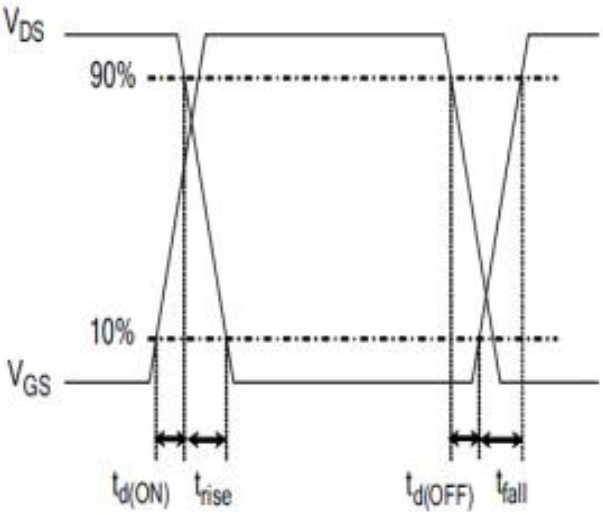


Figure13.
Resistive Switching Waveforms

Copyright Reasunos

Test Circuits and Waveforms

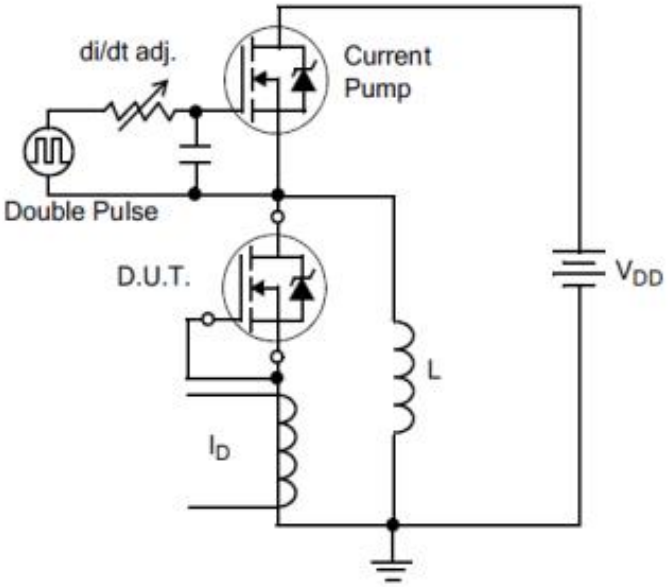


Figure14.Diode Reverse Recovery Test Circuit

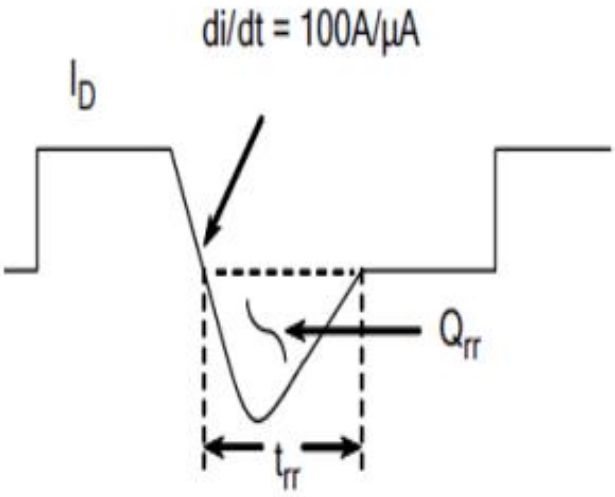


Figure15.Diode Reverse Recovery Waveform

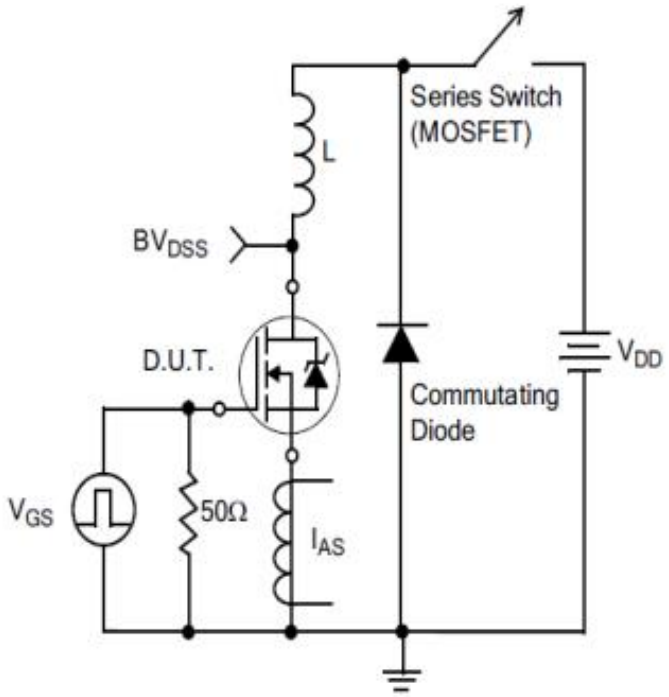
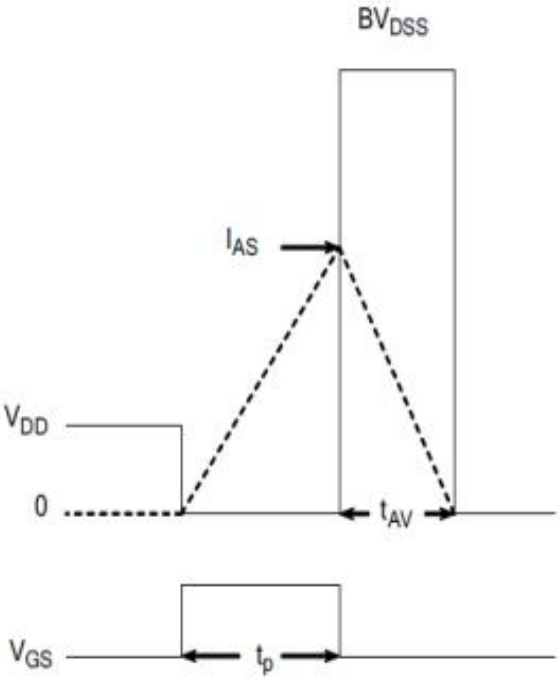


Figure16.Unclamped Inductive Switching Test Circuit

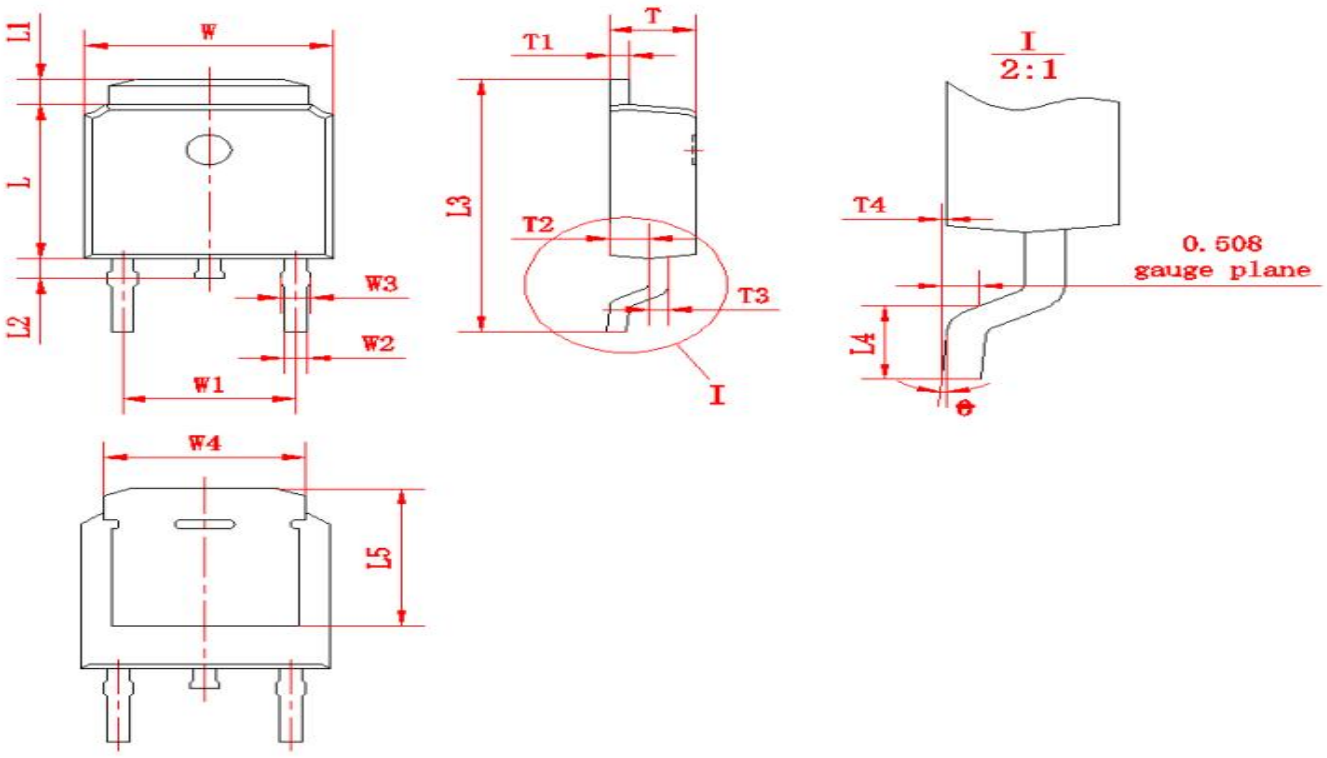


$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure17.Unclamped Inductive Switching Waveforms

Copyright Reasunos

Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

Copyright Reasunos

Disclaimers:

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights,nor the rights of others.Reproduction of inform- ation in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as cri- tical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.
As used herein:
1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,
c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.

Copyright Reasunos