# NCT6106D/ NCT6104D/ NCT6102D Application Note 2.8

## Feature Brief

NCT6106D/ NCT6104D/ NCT6102D: LPC I/F + UART + Parallel Port + KBC + ACPI + Hardware Monitor + GPIOs + PECI + DSW logic + AMDTSI + ERP

## Subject

This application note is applicable to all version chips except for the explicitly specified ones.

## Description

### 1. Layout for Temperature Detection Pin

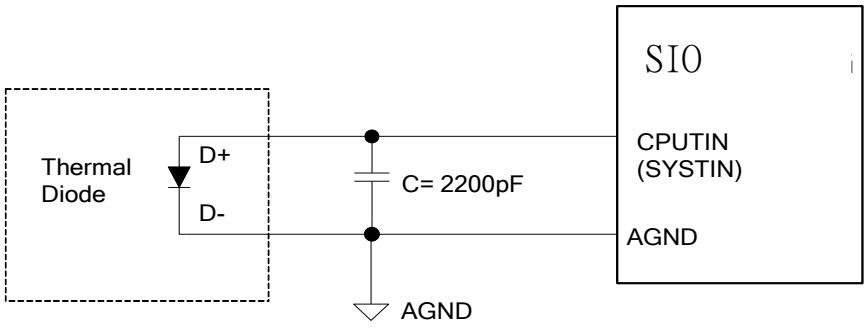
Since the NCT6106D/NCT6104D/NCT6102D supports remote diode temperature sensing through Current Mode, the layout is one of the important factors. The following items should be handled with care. Please pay attention to the following steps.

1) Place the NCT6106D/NCT6104D/NCT6102D closely to the thermal diode of the processor. The traces of D+ and D- should be as short and parallel as possible.

2) Put the recommended 2200pF capacitor between NCT6106D/NCT6104D/NCT6102D's CPUTIN (pin103) and AGND (pin105) as close as possible.

3) Pin105 of the NCT6106D/NCT6104D/NCT6102D is also an analog GND for ADC of H/W Monitor block; therefore, please separate it from normal power GND.

The circuit is shown in the following figure.



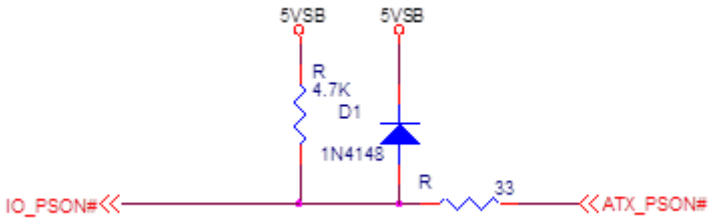

### 2. Battery power consumption

To save the battery power at pin74, please connect CASEOPEN# (pin76) to VBAT (pin74) with a 2M ohm pulled-up resistor if CASEOPEN function is not in use.

## 3. EOS damages resulted from pin72 (PSON#)

To avoid EOS damages to pin72 (PSON#), following protection circuit is recommended.

Add R (serial resister) and D1 (EOS protection diode) to avoid this issue on pin72 (PSON#).




## 4. Deal with unused input pins

Keep a fixed level on unused input pins to minimize the power consumption.

## 5. Unused PECI pin

SIO PECI pin could be floated if it is unused.

## 6. A 4.7uF bypass capacitor is added with VREF (pin102)

Since all of the monitored inputs are converted to digital values by a built-in, eight-bit analog-to-digital converter (ADC) of the NCT6106D/NCT6104D/NCT6102D and the VREF value is used as a reference voltage for this ADC. For better accuracy of the monitored inputs, adding a 4.7uF capacitor to AGND (pin 105) is needed.

## 7. 14.7456MHZ_CLKIN (pin108)

SIO UART have four source clocks can be selected. In UART clock 14.769 MHz, SIO NCT6106D/NCT6104D/NCT6102D has two clock sources, one is internal clock (24MHz / 1.625), another one is external clock from pin108 14.7456MHZ_CLKIN. In order to get better UART frequency accuracy, it's recommended to use external clock input (14.7456MHZ_CLKIN - pin108). Please note pin108 default function is GP67, BIOS can switch this pin to 14.7456MHZ_CLKIN function later.

## 8. Watch Dog Timer Application

Please be noted that the Watch Dog Timer function is enabled by default in NCT6106D/NCT6104D/NCT6102D. This is located at Logical Device 8, CR [30h], bit [0]. The unit of Watch Dog Timer counter can be selected at Logical Device 8, CR [F0h], bit [3]. The time-out value is set at Logical Device 8, CR [F1h], and the default is 4 sec. Writing a zero to this register disables the Watch Dog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watch Dog Timer counter and start counting down. It is reset by either LRESET# signal (default) or PWROK signal.

## 9. DC Fan Output Application

Please be noted that the maximum voltage of DC output mode of all fan control pins (SYSFANOUT, CPUFANOUT, and AUXFANOUT) is 2.048V in NCT6106D / NCT6104D / NCT6102D.

## 10. Intel DSW function Application

To use NCT6106D/NCT6104D/NCT6102D DSW pins, the following hardware and software application note should be followed.

Table 1 defines and explains the power well name for Intel DSW application. It also describes their existence (V or X) of each system states.

| POWER SOURCE | DESCRIPTION | DSW (DEEP S5/S4) | S5/S4 | S3 |
|---|---|---|---|---|
| V5A | 5V always power from ATX Power Supply | V | V | V |
| V3A | V5A will output a 3.3V always power via LDO or PWM Power IC.<br>The power will be provide to NCT610XD VSB power pin and PCH VCCDSW3_3 power pin. | V | V | V |
| 5VSB | 5V Suspend power, it will be cut in DSW state. | X | V | V |
| 3VSB | 3.3V Suspend Power, it will be cut in DSW state.<br>The Power will provide to PCH VCCSUS3_3 power pin.<br>NCT610XD PCHVSB pin will detect the 3VSB power via 1kohm resistor. | X | V | V |
| 5VDUAL | 5V Dual power, like USB power source. | X | Option | V |

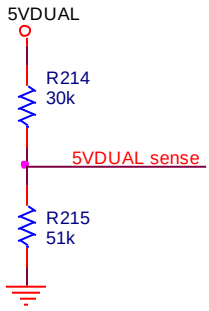
Table 1.

Table 2 shows NCT6106D/NCT6104D/NCT6102D DSW pins' name and characteristics, and recommended pull-up power well.

| PIN | NCT610XD PIN NAME | CONNECT TO INTEL PCH | POWER DETECT | POWER CONTROL | PULL-UP POWER SOURCE |
|---|---|---|---|---|---|
| 81 | SLP_SUS# | SLP_SUS# | | | |
| 83 | SUSACK# | SUSACK# | | | 3VSB |
| 85 | SUSWARN# | SUSWARN# | | | |
| 67 | PSOUT# | PWRBTN# | | | V3A |
| 75 | RSMRST# | RSMRST# | | | 3VSB |
| 84 | 5VDUAL | | SYSTEM 5VDUAL | | 5VDUAL power must be scaled down to 3V for detection. Note 1 |
| 69 | PCHVSB | | SYSTEM 3VSB | | 3VSB (1Kohm) |
| 80 | SLP_SUS_FET | | | Control 5VSB/3VSB power switch<br>0: Turn ON VSB<br>1: Turn OFF VSB | 5VSB |
| 82 | SUSWARN_5VDUAL | | | Control 5VDUAL power switch<br>0: Turn ON 5VDUAL<br>1: Turn OFF 5VDUAL | 5VSB |

Note 1.

5VDUAL power should be scaled to 3V by divided resistors as the following diagram. 5VDUAL_sense is connected to NCT6106D / NCT6104D / NCT6102D 5VDUAL pin (pin84).




Logical Device 16 CR30h bit3 and bit 6 must be set to 1 by BIOS.

### 23.22 Logical Device 16 (DEEP SLEEP)

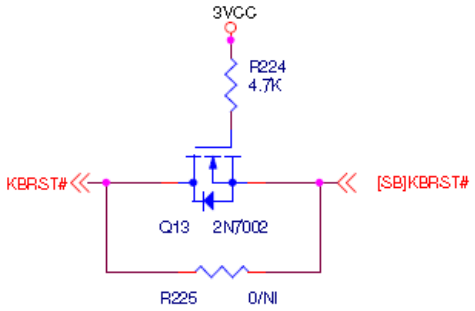
**CR 30h. Deep Sleep configuration register**

Location: Address 30h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 20h
Size: 8 bits

| | | |
|---|---|---|
| 6 | R / W | Set to 0, the RSMRST_SYS detect PSOUT# voltage.<br>Set to 1, the RSMRST_SYS detect PCHVSB voltage. |
| 3 | R / W | PCH_DSW_EN<br>Set to 0, if PCH disable DSW (Deep Sleep Well) function.<br>Set to 1, if PCH enable DSW (Deep Sleep Well) function. |

## 11. KBRST# and GA20M function Application

KBRST# and GA20M pins will be high level after 3VSB supplied by NCT6106D/NCT6104D /NCT6102D push-pull output logic. Please implement an isolation with 3VCC to avoid the leakage before system on.




## 12. Watch Dog Timer Accuracy

When the Watch Dog Timer setting is less than 15 sec, it is suggested that BIOS compensate 1~2 sec for more accuracy. For example, if the target Watch Dog Timer is 10 sec, BIOS needs to set it as 8 sec to compensate for the accuracy.

## 13. UART RS485 Auto Flow Control

**[For rev. B]**
NCT6102D / NCT6104D / NCT6106D supports RS485 auto flow control function for all UART. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for flow control.
To make this RS485 auto flow control function work, please be noted that the parity and stop-bit setting has to be one of the following three settings:
(1) 8 data bits + 1 parity bit + 1 stop bit
(2) 8 data bits + 1 parity bit + 2 stop bits
(3) 8 data bits + 2 stop bits

**[For rev. C]**
To make this RS485 auto flow control function work, please set either

8 data bits + 1 stop bit

Or one of the following three settings:

(1) 8 data bits + 1 parity bit + 1 stop bit
(2) 8 data bits + 1 parity bit + 2 stop bits
(3) 8 data bits + 2 stop bits

## 14. Status of UARTs output pins while UARTs are inactive

UART output pins are SOUT, RTS#, and DTR#.
When UART ports are inactive, the status of the UART output pins are tri-state by default. To keep the status of the UART output pins logic high, please reserve the pull-up resisters for the UART output pins.
For those UART output pins that are related to strapping functions, it needs BIOS to change the strapping value to high by CR 26h and CR 2Fh in Chip (Global) Control Register if these pins are strapped low.
However, for pin #51 or RTSA# (2E_4E_SEL), if it is strapped low for SIO address selection, then please keep UART A active so that the RTSA# output will be high.

| Pin Number | Pin Names | Strapping Function |
|---|---|---|
| 51 | RTSA# | 2E_4E_SEL |
| 52 | DTRA# | 24M_48M_SEL |
| 54 | SOUTA | GPIO_PORT80_SEL |
| 111 | RTSC# | SOUTC_P80_SEL |
| 112 | DTRC# | SOUTE_P80_SEL |

**CR 26h. Global Option** s: value by strapping
Location: Address 26h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : by 0s00_0000
Size: 8 bits

| BIT | READ / WRITE | DESCRIPTION |
|---|---|---|
| 7 | Reserved. | |
| 6 | R / W | HEFRAS =><br>= 0 Write 87h to location 2E twice.<br>= 1 Write 87h to location 4E twice.<br>The corresponding power-on strapping pin is RTSA# (Pin51). |

**CR 2Fh. Strapping Function Result**

Location: Address 2Fh
Attribute: Read/Write
Power Well: VSB
Reset by: PWROK#, RSMRST# (Bit2)
Default : by 000s_ssss
Size: 8 bits

| BIT | READ / WRITE | DESCRIPTION |
|---|---|---|
| 7-5 | Reserved. | |
| 4 | R / W | SOUTE_P80_SEL Strapping result reading, it can output the port80 data to UARTE interface. |
| 3 | R / W | SOUTC_P80_SEL Strapping result reading, it can output the port80 data to UARTE interface. |
| 2 | R / W | COMB_DSW_SEL Strapping result reading, it can switch UARTB pad-mux to DSW function. |
| 1 | R / W | GPIO_PORT80_SEL Strapping result reading |
| 0 | R / W | 24M_48M_SEL Strapping result reading |

## NCT6106D / NCT6104D / NCT6102D Application Note

| DATE | DOCUMENT | REVISION | REMARK |
|---|---|---|---|
| 11/09/2011 | APN | 1.0 | First release. |
| 05/28/2012 | APN | 2.0 | Add Watch Dog Timer application and fan DC mode application |
| 10/05/2012 | APN | 2.1 | Add DSW function application |
| 10/26/2012 | APN | 2.2 | Added KBRST# function application. |
| 03/28/2013 | APN | 2.3 | Add Watch Dog Timer accuracy |
| 05/10/2013 | APN | 2.4 | Update item 9, item 11 and add item 13 |
| 05/20/2013 | APN | 2.5 | Remove unnecessary note in item 9 -- DC Fan Output Application |
| 09/10/2013 | APN | 2.6 | Add NCT6104D and NCT6102D in the APN |

| DATE | DOCUMENT | REVISION | REMARK |
|---|---|---|---|
| 10/17/2014 | APN | 2.7 | Status of UARTs output pins while UARTs are inactive |
| 11/10/2014 | APN | 2.8 | Update item #13, UART Auto Flow Control application for both rev. B and rev. C |