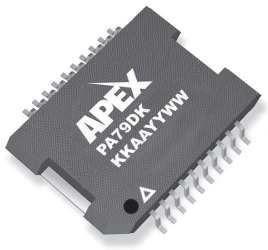
PA79

Power Operational Amplifier

RoHS COMPLIANT

FEATURES



- A Unique (Patent Pending) Technique for Very Low Quiescent Current
- Over 350 V/µs Slew Rate
- Wide Supply Voltage
  - Single Supply: 20V To 350V
  - Split Supplies: ± 10V To ± 175V
- Output Current – Per Amplifier – 50mA Cont.; 200mA Pk
- Up to 26 Watt Dissipation Capability (Dual)
- Over 200 kHz Power Bandwidth

APPLICATIONS

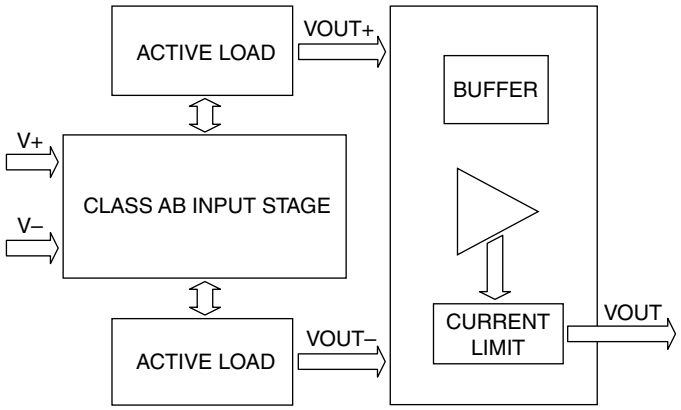
- Piezoelectric Positioning and Actuation
- Electrostatic Deflection
- Deformable Mirror Actuators
- Chemical and Biological Stimulators

DESCRIPTION

The PA79 is a high voltage, high speed, low idle current op-amp capable of delivering up to 200mA peak output current. Due to the dynamic biasing of the input stage, it can achieve slew rates over 350V/µs, while only consuming less than 1mA of idle current. External phase compensation allows great flexibility for the user to optimize bandwidth and stability.

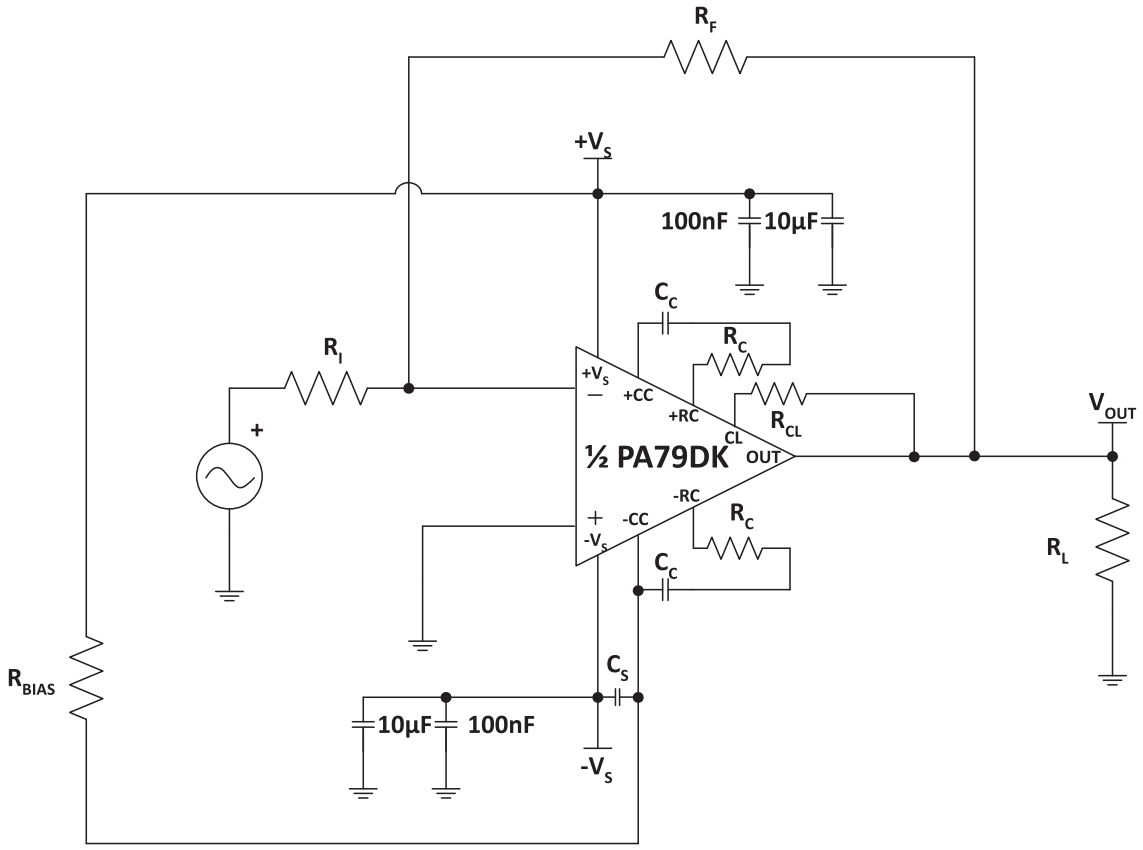
The output stage is protected with user selected current limit resistor. For the selection of this current limiting resistor, pay close attention to the SOA curves for each package type. Proper heatsinking is required for maximum reliability.

Figure 1: Equivalent Schematic



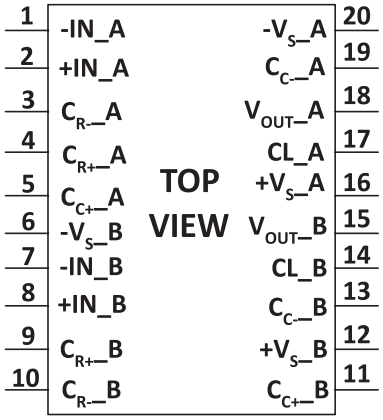
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Notes:

1. The package heat slug needs to be connected to a stable reference such as gnd for high slew rates. Please refer to special considerations section for details.
2. Supply bypassing required for $-V_S$ and $+V_S$.
3. For C_C and R_C values refer to power supply biasing section.
4. Dimple and ESD triangle denotes pin 1.

Pin Number	Name	Description
1	-IN_A	The inverting input for channel A.
2	+IN_A	The non-inverting input for channel A.
3	-RC_A	Negative compensation resistor connection for channel A. Select value based on Phase Compensation. See applicable section.
4	+RC_A	Positive compensation resistor connection for channel A. Select value based on Phase Compensation. See applicable section.
5	+CC_A	Positive compensation capacitor connection for Channel A. Select value based on Phase Compensation. See applicable section.
6	-Vs_B	The negative supply rail for channel B.
7	-IN_B	The inverting input for channel B.
8	+IN_B	The non-inverting input for channel B.
9	+RC_B	Positive compensation resistor connection for channel B. Select value based on Phase Compensation. See applicable section.
10	-RC_B	Negative compensation resistor connection for channel B. Select value based on Phase Compensation. See applicable section.
11	+CC_B	Positive compensation capacitor connection for channel B. Select value based on Phase Compensation. See applicable section.
12	+Vs_B	The positive supply rail for channel B.
13	-CC_B	Negative compensation capacitor connection for channel B. Select value based on Phase Compensation. See applicable section.

Pin Number	Name	Description
14	CL_B	Connect to the current limit resistor. Output current flows into/out of these pins through R_{CL_B}. The output pin and the load are connected to the other side of the R_{CL_B}.
15	OUT_B	The output for channel B. Connect this pin to load and to the feedback resistors.
16	+Vs_A	The positive supply rail for channel A.
17	CL_A	Connect to the current limit resistor. Output current flows into/out of these pins through R_{CL_A}. The output pin and the load are connected to the other side of the R_{CL_A}.
18	OUT_A	The output for channel A. Connect this pin to load and to the feedback resistors.
19	-CC_A	Negative compensation capacitor connection for channel A. Select value based on Phase Compensation. See applicable section.
20	-Vs_A	The negative supply rail for channel A.

SPECIFICATIONS

Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given, power supply voltage is typical rating.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_s$ to $-V_s$		350	V
Output Current, peak (200ms), within SOA	I_O		200	mA
Power Dissipation, internal, DC Single	P_D		14	W
Power Dissipation, internal, DC Dual	P_D		26	W
Input Voltage, differential	$V_{IN\ (Diff)}$	-15	15	V
Input Voltage, common mode	V_{cm}	$-V_S$	V_S	V
Temperature, junction [1]	T_J		150	°C
Temperature Range, storage		-55	125	°C
Operating Temperature Range, case	T_C	-40	85	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.

INPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Offset Voltage, initial		-40	8	40	mV
Offset Voltage vs. temperature	0 to 125°C (Case Temperature)		-63		µV/°C
Offset Voltage vs. supply				32	µV/V
Bias Current, initial			8.5	200	pA
Offset Current, initial			12	400	pA
Input Resistance, DC [1]			10^8		Ω
Common Mode Voltage Range, pos.			$+V_S$ - 2		V
Common Mode Voltage Range, neg.			$-V_S$ + 5.5		V
Common Mode Rejection, DC		90	118		dB
Noise	700 kHz		418		µV RMS
Noise, V_O Noise			500		nV/√Hz

1. Rating applies when power dissipation is equal in two amplifiers.

GAIN

Parameter	Test Conditions	Min	Typ	Max	Units
Open Loop @ 1 Hz		89	120		dB
Gain Bandwidth Product @ 1 MHz			1		MHz
Phase Margin	Full temp range		50		°

OUTPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage Swing	I_O = 10mA		$\|V_S\|$ - 2		V
Voltage Swing	I_O = 100mA		$\|V_S\|$ - 8.6	$\|V_S\|$ - 12	V
Voltage Swing	I_O = 150mA		$\|V_S\|$ - 10		V
Current, continuous, DC		150			mA
Slew Rate	Package Tab connected to GND	100	350		V/µs
Settling Time to 0.1%	5V Step (No Compensation)		1		µs
Power Bandwidth, $300V_{P-P}$	$+V_S$ = 160V, $-V_S$ = -160V		200		kHz
Output Resistance, no load	R_{CL} = 6.2 Ω		44		Ω

POWER SUPPLY

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage		±10	±150	±175	V
Current, quiescent[1]	±150V Supply	0.2	0.7	2.5	mA

1. Supply current increases with signal frequency. See Figure 32. Applies to each amplifier.

THERMAL

Parameter	Test Conditions	Min	Typ	Max	Units
Resistance, DC, junction to case, Dual [1]	Full temp range		5.5		°C/W
Resistance, DC, junction to case, Single	Full temp range		8.3	9.1	°C/W
Resistance, junction to air, Dual	Full temp range		25		°C/W
Resistance, junction to air, Single	Full temp range		19.1		°C/W
Temperature Range, case		-40		125	°C

1. Rating applies when power dissipation is equal in two amplifiers.

Notes:

1. $+V_S$ and $-V_S$ denote the positive and negative supply voltages of the output stage.
2. Rating applies if output current alternates between both output transistors at a rate faster than 60 Hz.
3. Rating applies when the heatslug of the DK package is soldered to a minimum of 1 square inch foil area of a printed circuit board.
4. Rating applies with the JEDEC conditions outlined in the Heatsinking section of this datasheet.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Response

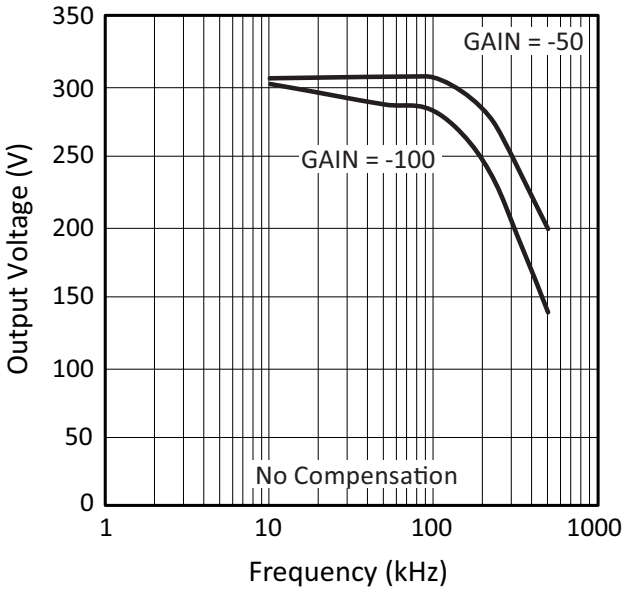


Figure 5: Current Limit

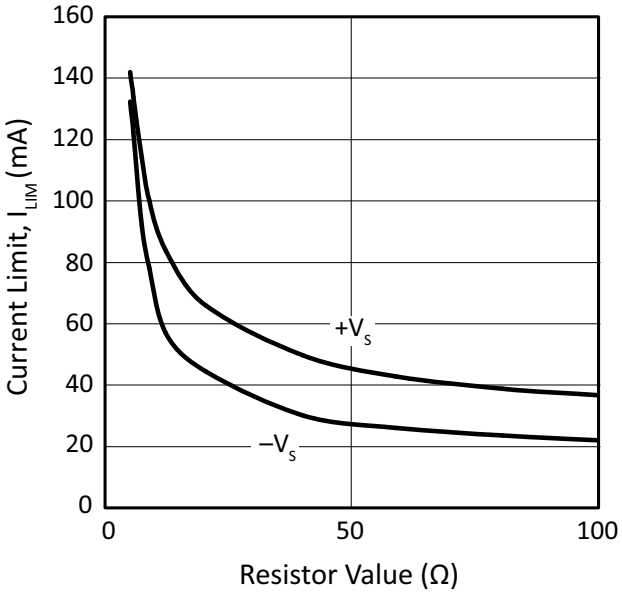


Figure 6: Power Derating

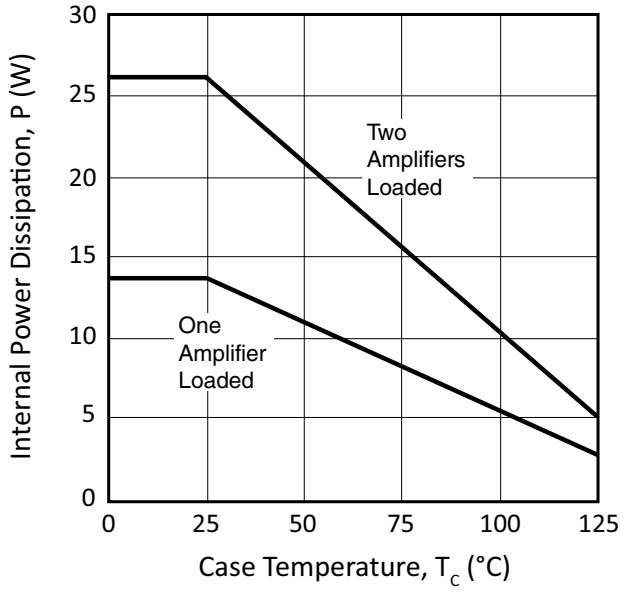


Figure 7: Power Supply Rejection

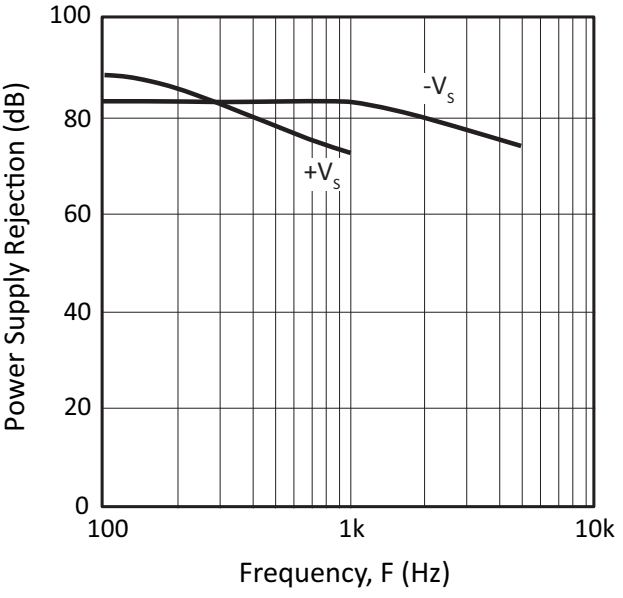


Figure 8: Output Voltage Swing

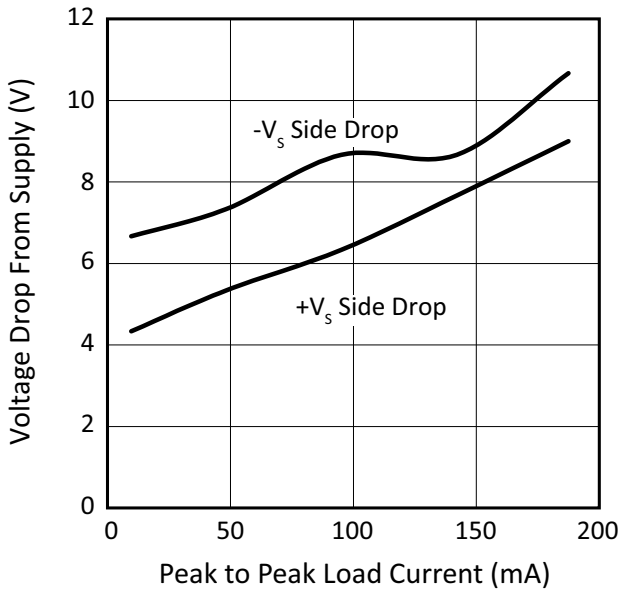


Figure 9: Common Mode Rejection

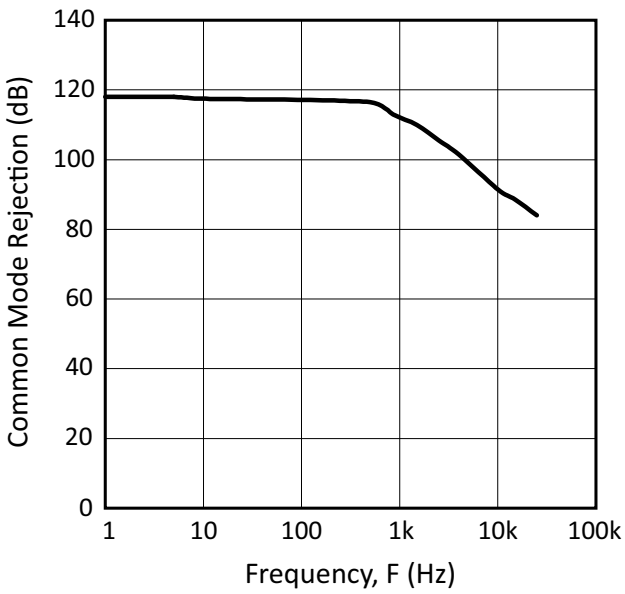


Figure 10: Open Loop Gain

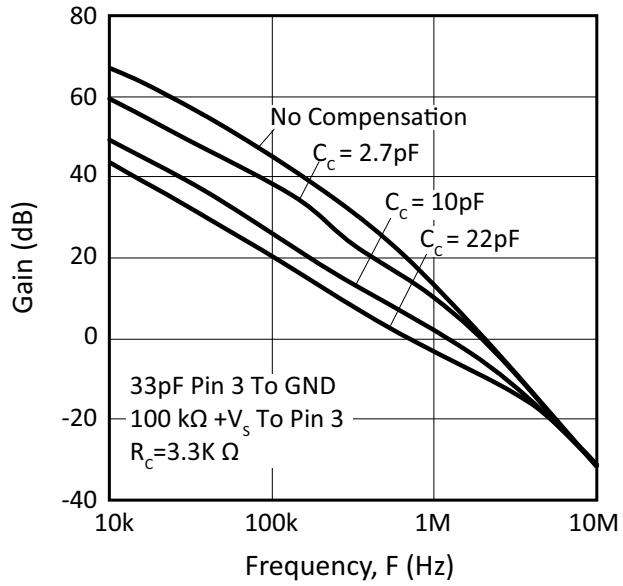


Figure 11: Phase Response

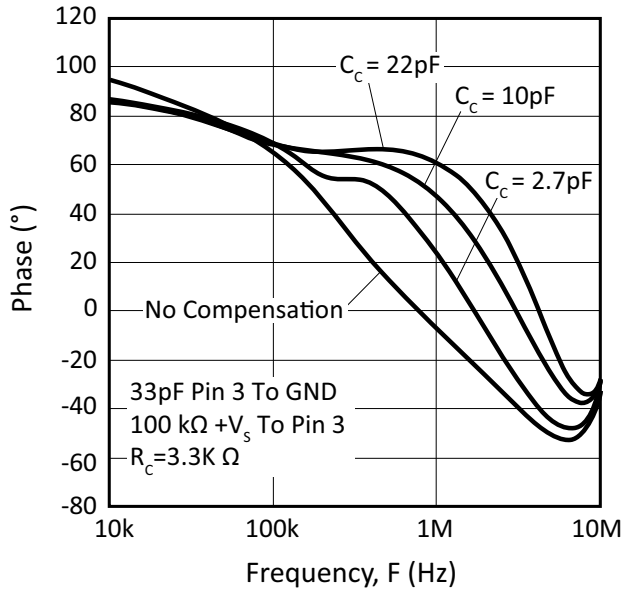


Figure 12: Small Signal Open Loop Gain

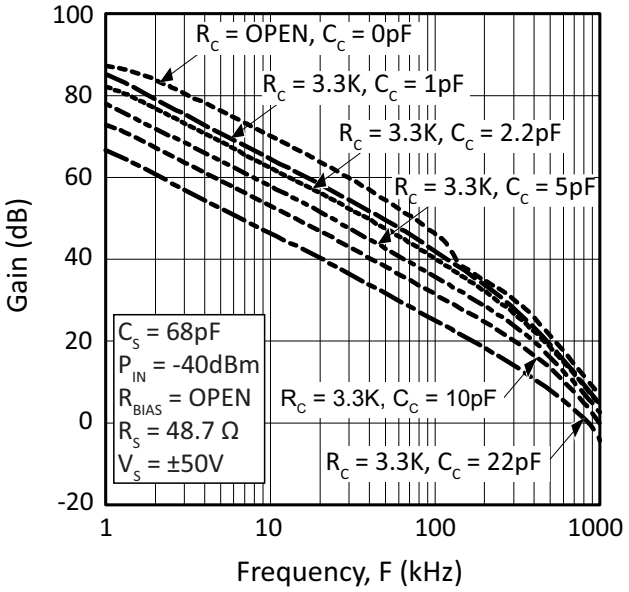


Figure 13: Gain vs. Input/Output Signal Level

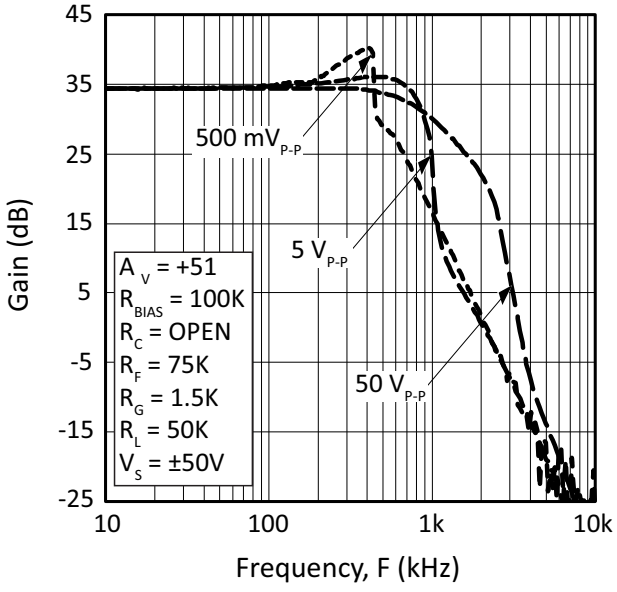


Figure 14: Small Signal Open Loop Phase, $V_O = 250mV_{P-P}$

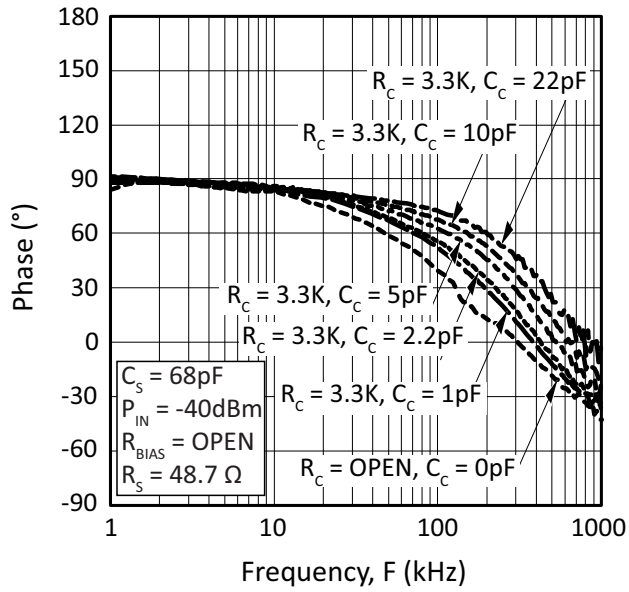


Figure 15: Small Signal Gain vs. Compensation, $V_O = 500mV_{P-P}$

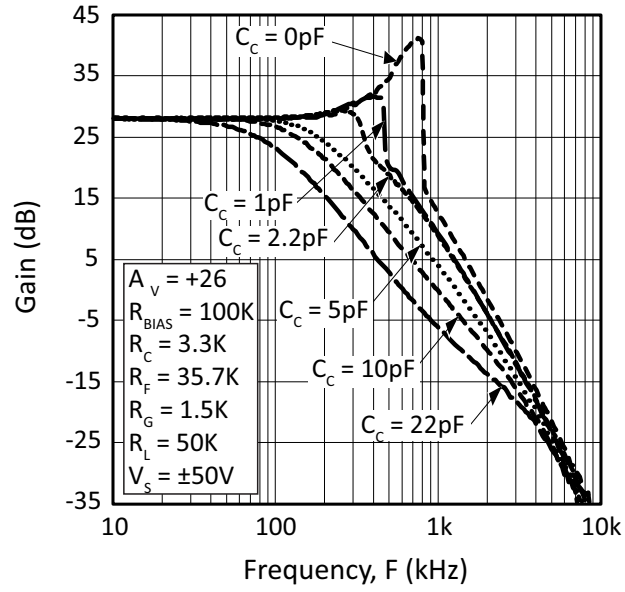


Figure 16: Small Signal Open Loop Phase

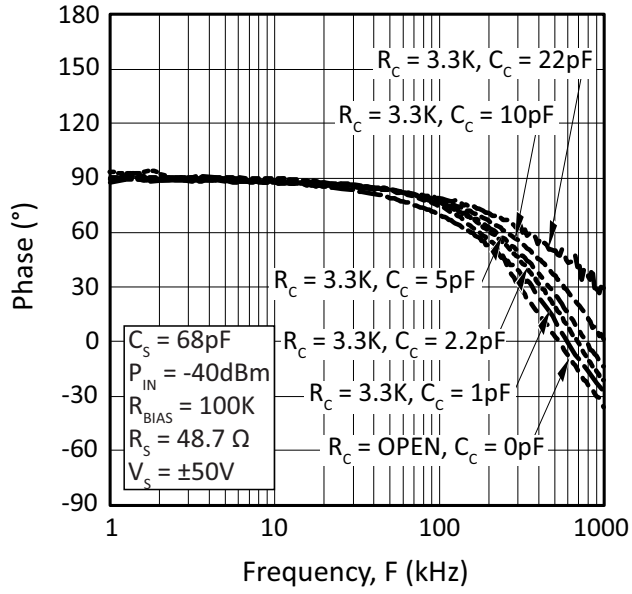


Figure 17: Small Signal Gain vs. Compensation, $V_O = 5V_{P-P}$

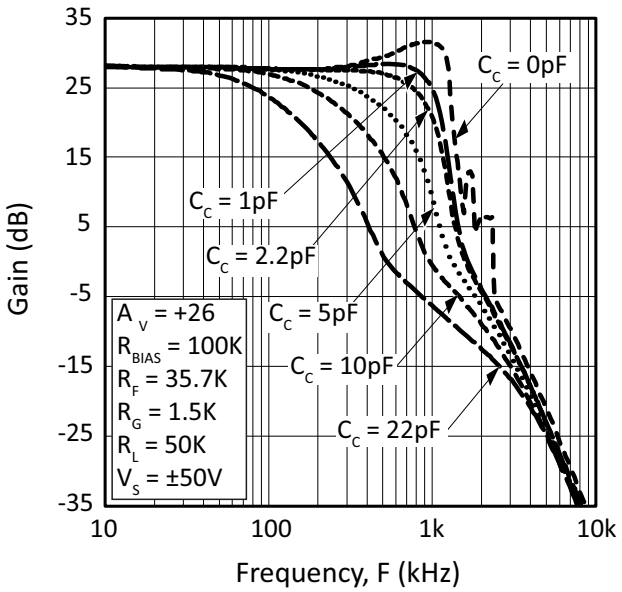


Figure 18: Large Signal Gain vs. Compensation, $V_O = 50V_{P-P}$

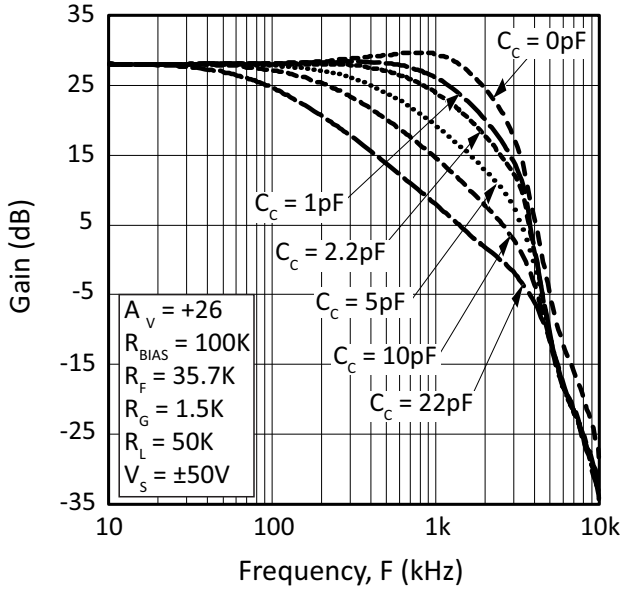


Figure 19: SR+/SR- (25% - 75%)

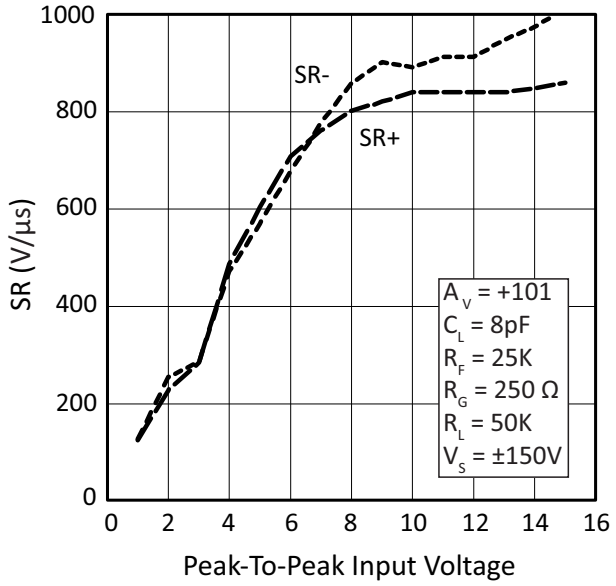


Figure 20: Transient Response

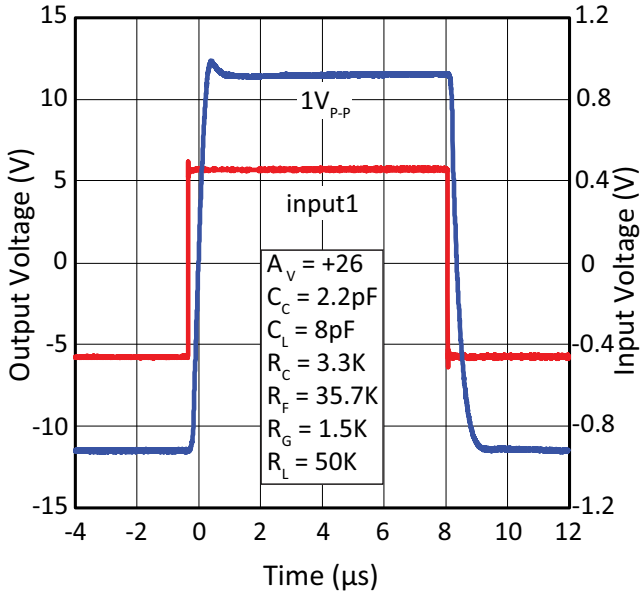


Figure 21: SR+/SR- (25% - 75%)

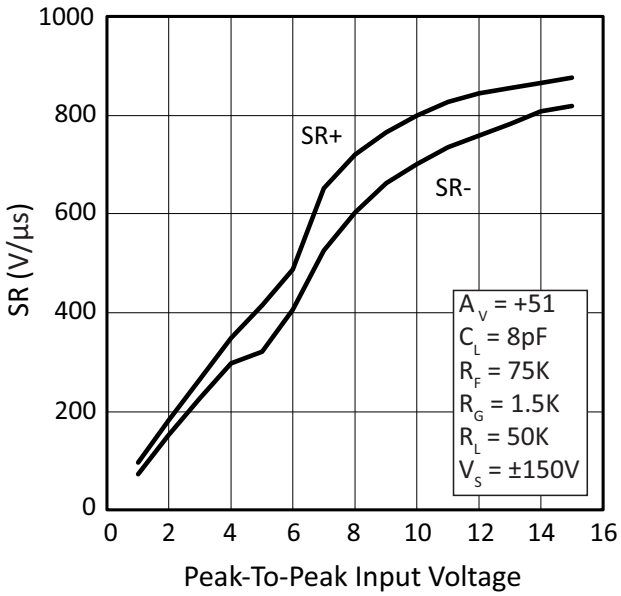


Figure 22: Transient Response

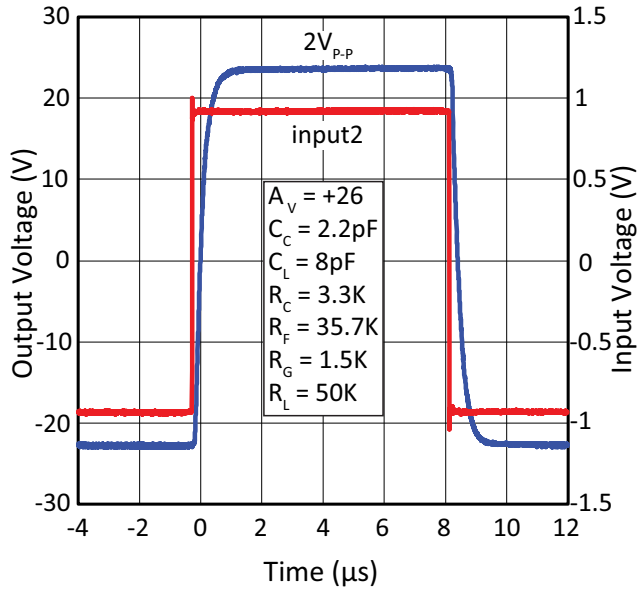


Figure 23: SR+/SR- (25% - 75%)

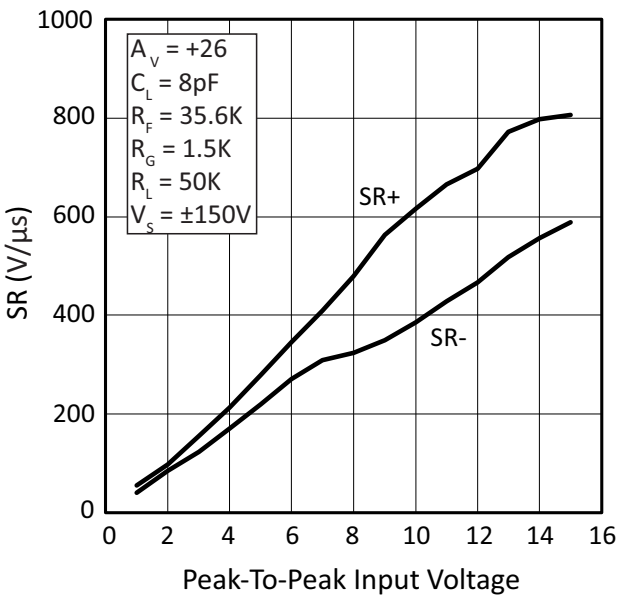


Figure 24: Transient Response

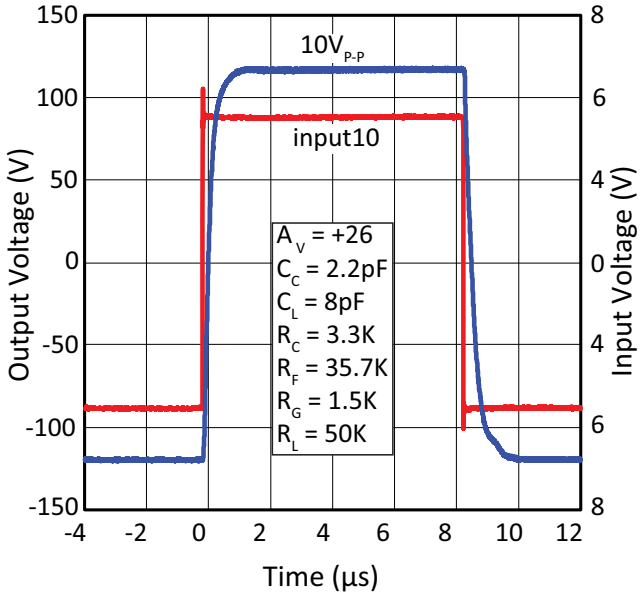


Figure 25: Rise and Fall Time (10% - 90%)

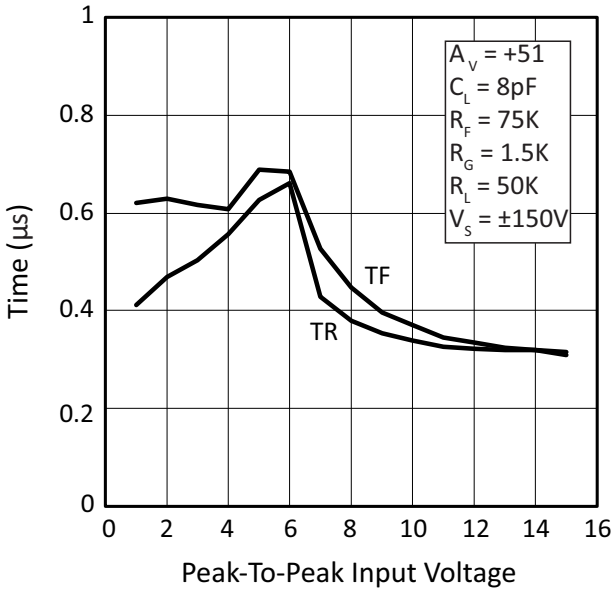


Figure 26: Pulse Response vs. C_C and R_C

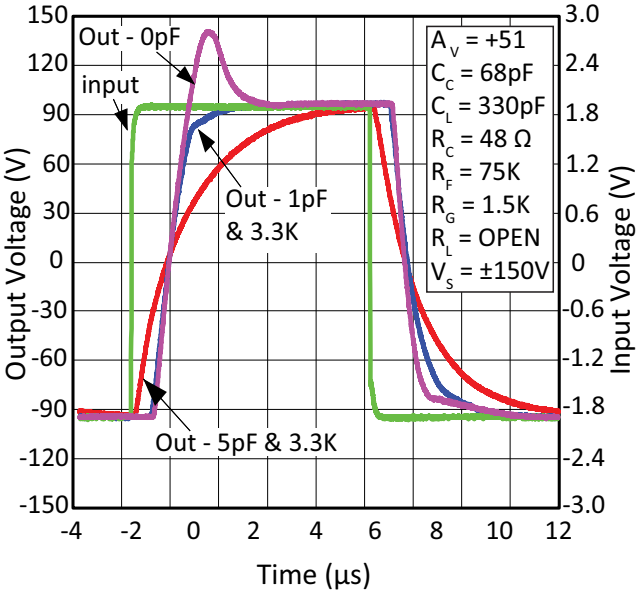


Figure 27: Pulse Response vs. Cap Load

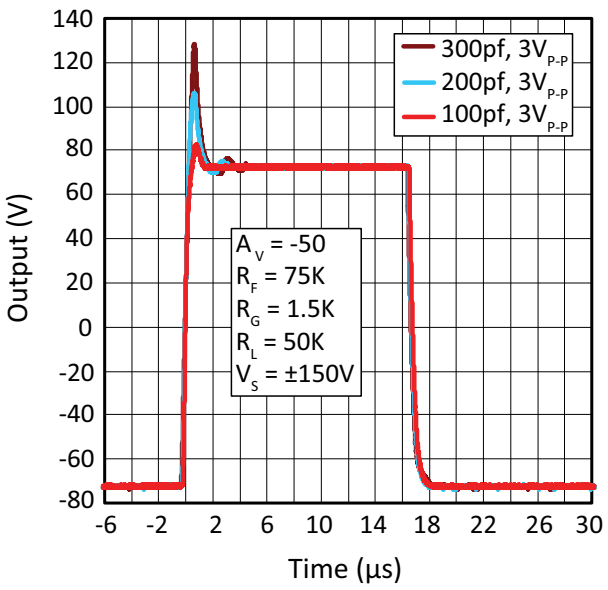


Figure 28: Pulse Response

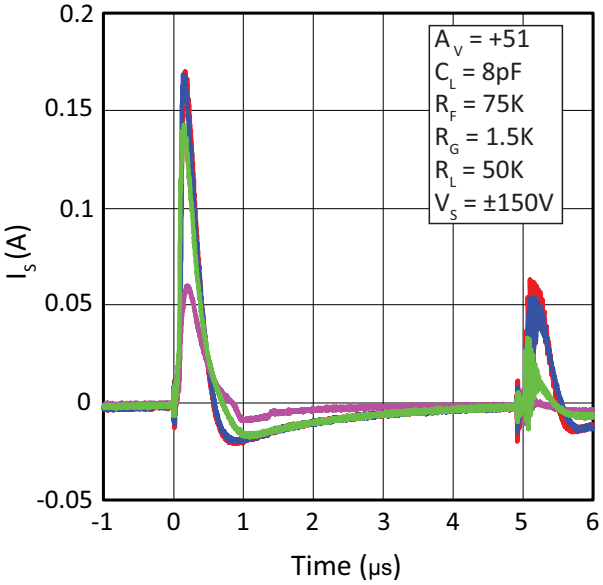


Figure 29: Pulse Response vs. Cap Load

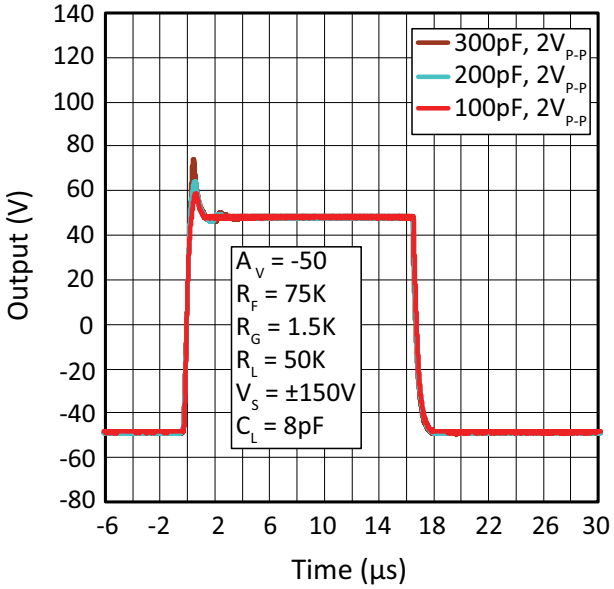


Figure 30: Overdrive Recovery

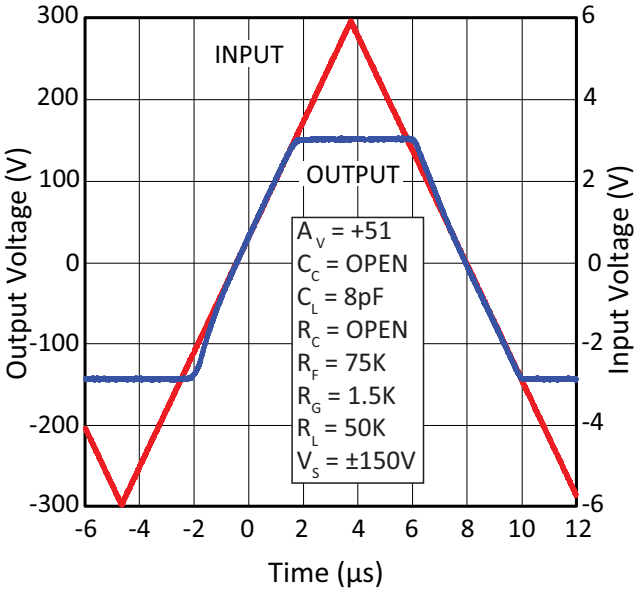


Figure 31: Pulse Response vs. Cap Load

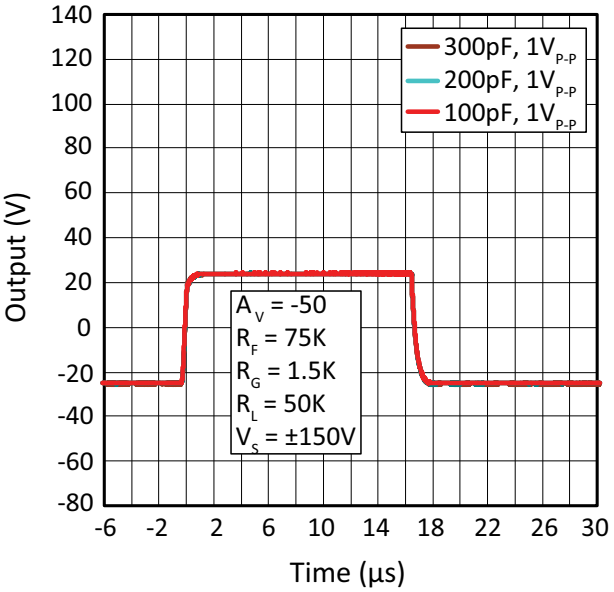


Figure 32: I_S vs. V_{IN}

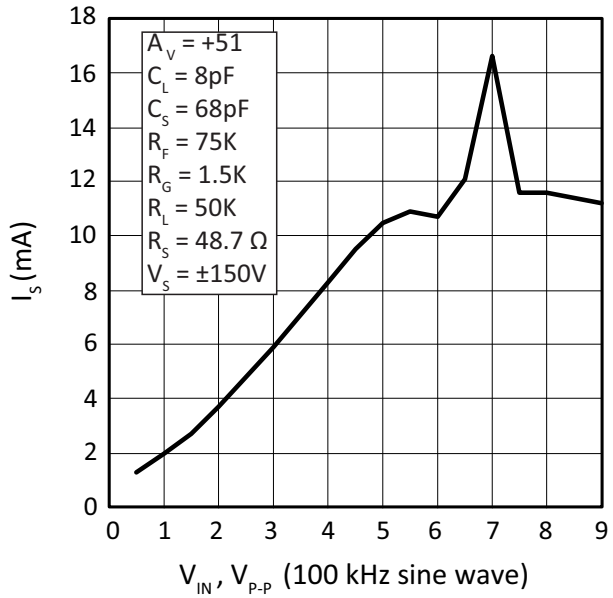


Figure 33: Supply Current vs. Frequency

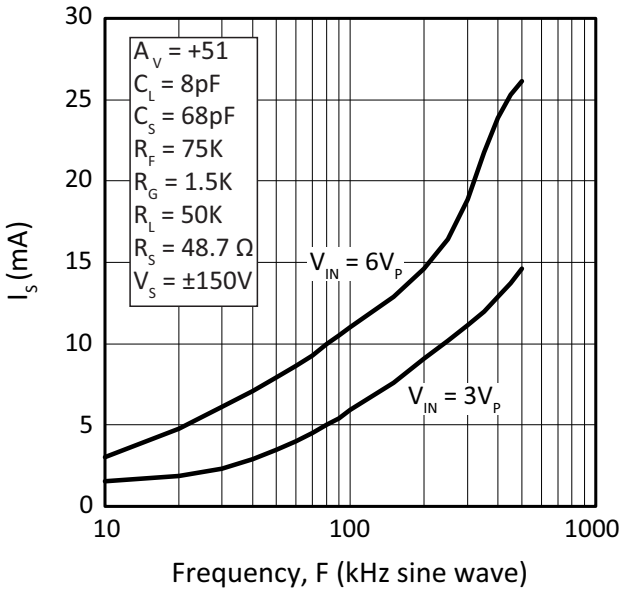


Figure 34: SR+/SR- (25%-75%)

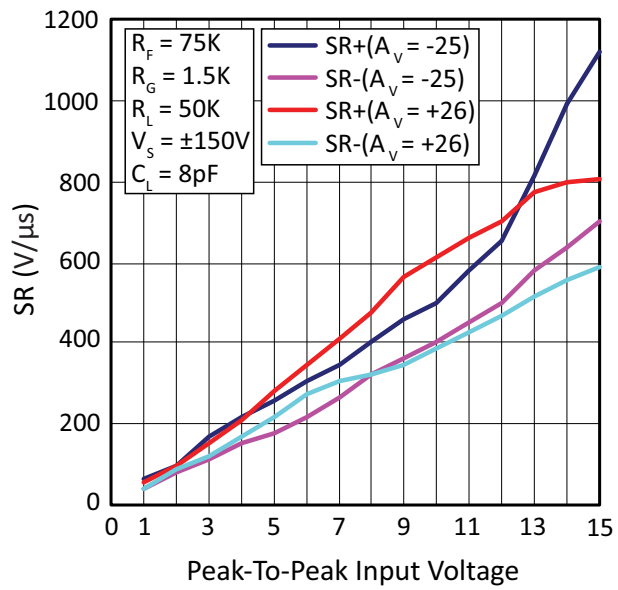
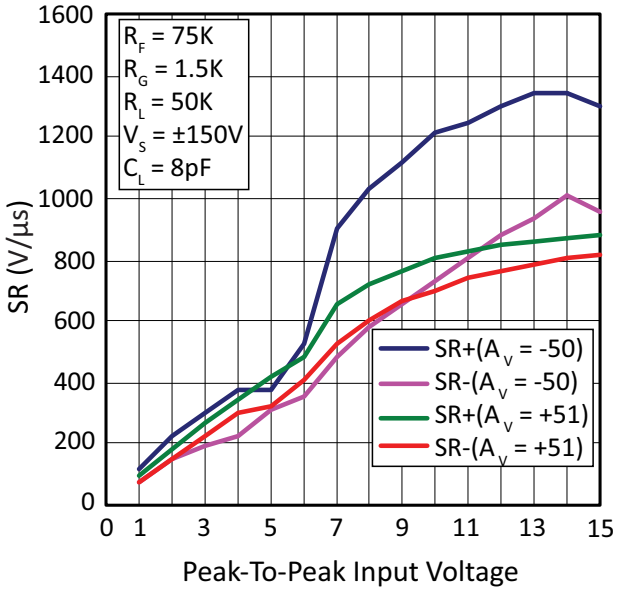


Figure 35: SR+/SR- (25%-75%)



SAFE OPERATING AREA (SOA)

Figure 36: Single Amplifier SOA

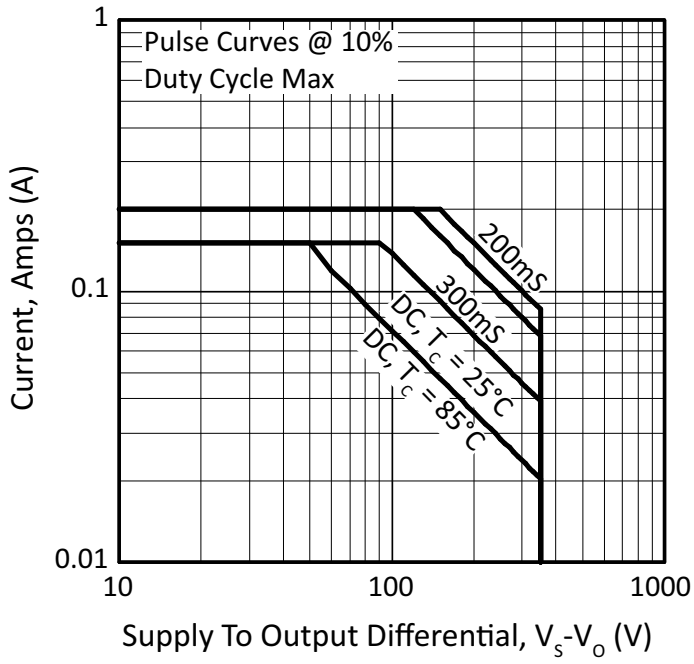
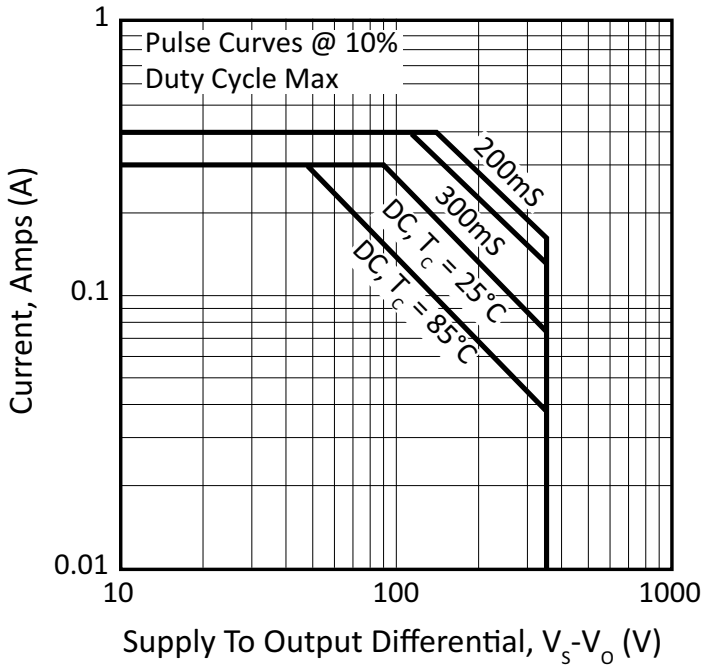


Figure 37: Dual Amplifier SOA



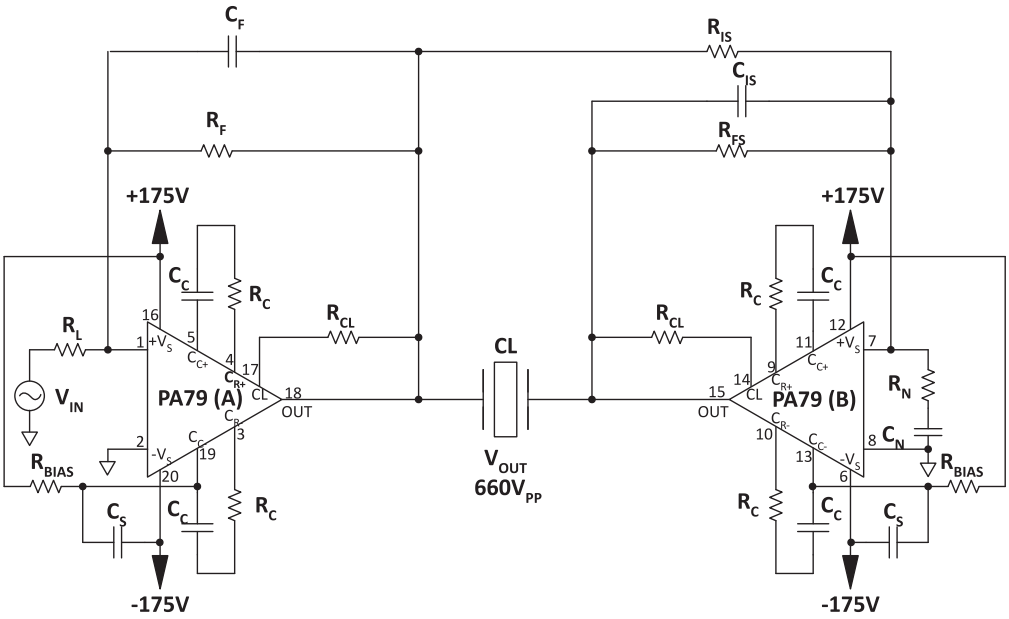
GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION CIRCUIT

The PA79 is ideally suited for driving continuous drop ink jet printers, in both Piezo actuation and deflection applications. The high voltage of the amplifier creates an electrostatic field on the deflection plates to control the position of the ink droplets. The rate at which droplets can be printed is directly related to the rate at which the amplifier can drive the plate to a different electrostatic field strength.

Figure 38: Typical Application



THEORY OF OPERATION

The PA79 is designed specifically as a high speed pulse amplifier. In order to achieve high slew rates with low idle current, the internal design is quite different from traditional voltage feedback amplifiers. Basic op amp behaviors like high input impedance and high open loop gain still apply. But there are some notable differences, such as signal dependent supply current, bandwidth and output impedance, among others. The impact of these differences varies depending on application performance requirements and circumstances. These different behaviors are ideal for some applications but can make designs more challenging in other circumstances.

SUPPLY CURRENT AND BYPASS CAPACITANCE

A traditional voltage feedback amplifier relies on fixed current sources in each stage to drive the parasitic capacitances of the next stage. These currents combine to define the idle or quiescent current of the amplifier. By design, these fixed currents are often the limiting parameter for slew rate and bandwidth of the amplifier. Amplifiers which are high voltage and have fast slew rates typically have high idle currents and dissipate notable power with no signal applied to the load. At the heart of the PA79 design is a signal dependent current source which strikes a new balance between supply current and dynamic performance. With small input signals, the supply current of the PA79 is very low, idling at less than 1 mA. With large transient input signals, the supply currents increase dramatically to allow the amplifier stages to respond quickly. The Pulse Response plot in the typical performance section of this datasheet describes the dynamic nature of the supply current with various input transients.

Choosing proper bypass capacitance requires careful consideration of the dynamic supply currents. High frequency ceramic capacitors of 0.1µF or more should be placed as close as possible to the amplifier supply pins. The inductance of the routing from the supply pins to these ceramic capacitors will limit the supply of peak current during transients, thus reducing the slew rate of the PA79. The high frequency capacitance should be supplemented by additional bypass capacitance not more than a few centimeters from the amplifier. This additional bypass can be a slower capacitor technology, such as electrolytic, and is necessary to keep the supplies stable during sustained output currents. Generally, a few microfarad is sufficient.

SMALL SIGNAL PERFORMANCE

The small signal performance plots in the typical performance section of this datasheet describe the behavior when the dynamic current sources described previously are near the idle state. The selection of compensation capacitor directly affects the open loop gain and phase performance.

Depending on the configuration of the amplifier, these plots show that the phase margin can diminish to very low levels when left uncompensated. This is due to the amount of bias current in the input stage when the part is in standby. An increase in the idle current in the output stage of the amplifier will improve phase margin for small signals although will increase the overall supply current.

Current can be injected into the output stage by adding a resistor, R_{BIAS}, between C_C- and V_S+. The size of R_{BIAS} will depend upon the application but 500µA (50V V+ supply/100K) of added bias current shows significant improvement in the small signal phase plots. Adding this resistor has little to no impact on small signal gain or large signal performance as under these conditions the current in the input stage is elevated over its idle value. It should also be noted that connecting a resistor to the upper supply only injects a fixed current and if the upper supply is fixed and well bypassed. If the application includes variable or adjustable supplies, a current source diode could also be used. These two terminal components combine a JFET and resistor connected within the package to behave like a current source.

As a second stability measure, the PA79 is externally compensated and performance can be optimized to the application. Unlike the R_{BIAS} technique, external phase compensation maintains the low idle current but does affect the large signal response of the amplifier. Refer to the small and large signal response plots as a guide in making the trade offs between bandwidth and stability. Due to the unique design of the PA79, two symmetric compensation networks are required. The compensation capacitor Cc must be rated for a working voltage of the full operating supply voltage ($+V_S$ to $-V_S$). NPO capacitors are recommended to maintain the desired level of compensation over temperature.

The PA79 requires an external 33pF capacitor between C_C- and $-V_S$ to prevent oscillations in the falling edge of the output. This capacitor should be rated for the full supply voltage ($+V_S$ to $-V_S$).

LARGE SIGNAL PERFORMANCE

As the amplitude of the input signal increases, the internal dynamic current sources increase the operation bandwidth of the amplifier. This unique performance is apparent in its slew rate, pulse response, and large signal performance plots. Recall the previous discussion about the relationships between signal amplitude, supply current, and slew rate. As the amplitude of the input amplitude increases from $1V_{P-P}$ to $15V_{P-P}$, the slew rate increases from 50V/µs to well over 350V/µs.

Notice the knee in the Rise and Fall times plot, at approximately $6V_{P-P}$ input voltage. Beyond this point the output becomes clipped by the supply rails and the amplifier is no longer operating in a closed loop fashion. The rise and fall times become faster as the dynamic current sources are providing maximum current for slewing. The result of this amplifier architecture is that it slews fast, but allows good control of overshoot for large input signals. This can be seen clearly in the large signal Transient Response plots.

HEATSINKING AND SAFE OPERATING AREA

The MOSFET output stage of the PA79 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations of the package and current handling capabilities limit the Safe Operating Area. The SOA plots include power dissipation limitations which are dependent upon case temperature. Keep in mind that the dynamic current sources which drive high slew rates can increase the operating temperature of the amplifier during periods of repeated slewing. The plot of supply current vs. input signal amplitude for a 100 kHz signal provides an indication of the supply current with repeated slewing conditions. This application dependent condition must be considered carefully.

The output stage is self-protected against transient flyback by the parasitic body diodes of the output stage. However, for protection against sustained high energy flyback, external, fast recovery diodes must be used.

CURRENT LIMIT

For proper operation, the current limit resistor, R_{LIM}, must be connected as shown in the external connections diagram. For maximum reliability and protection, the largest resistor value should be used. The minimum practical value for R_{LIM} is about 12 Ω. However, refer to the SOA curves for each package type to assist in selecting the optimum value for R_{LIM} in the intended application. Current limit may not protect against short circuit conditions with supply voltages over 200V.

LAYOUT CONSIDERATIONS

The PA79 is built on a dielectrically isolated process and the package tab is therefore not electrically connected to the amplifier. For high speed operation, the package tab should be connected to a stable reference to reduce capacitive coupling between amplifier nodes and the floating tab. It is often convenient to directly connect the tab to GND or one of the supply rails, but an AC connection through a 1µF capacitor to GND is also sufficient if a DC connection is undesirable. Care should be taken to position the R_C / C_C compensation networks close to the amplifier compensation pins. Long loops in these paths pick up noise and increase the likelihood of LC interactions and oscillations.

The PA79DK package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heat slug to a 1 square inch foil area on the printed circuit board will result in improved thermal performance of 25°C/W. In order to improve the thermal performance, multiple metal layers in the printed circuit board are recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85°C.

The junction to ambient thermal resistance of the DK package can achieve a 19.1°C/W rating by using the PCB conditions outlined in JEDEC standard: (JESD51–5):

PCB Conditions:
PCB Layers = 4L, Copper, FR–4
PCB Dimensions = 101.6 x 114.3mm
PCB Thickness = 1.6mm
Conditions:
Power dissipation = 2 watts
Ambient Temperature = 55°C

MOISTURE SENSITIVITY

The PA79DK has been qualified according to JEDEC 22-A-113-D, MSL 3. The following conditions were used: IR reflow for Pb-free assembly profile where: package thickness is greater than 2.5mm, package volume is greater than 350mm^2, TP = 245°C.

ELECTROSTATIC DISCHARGE

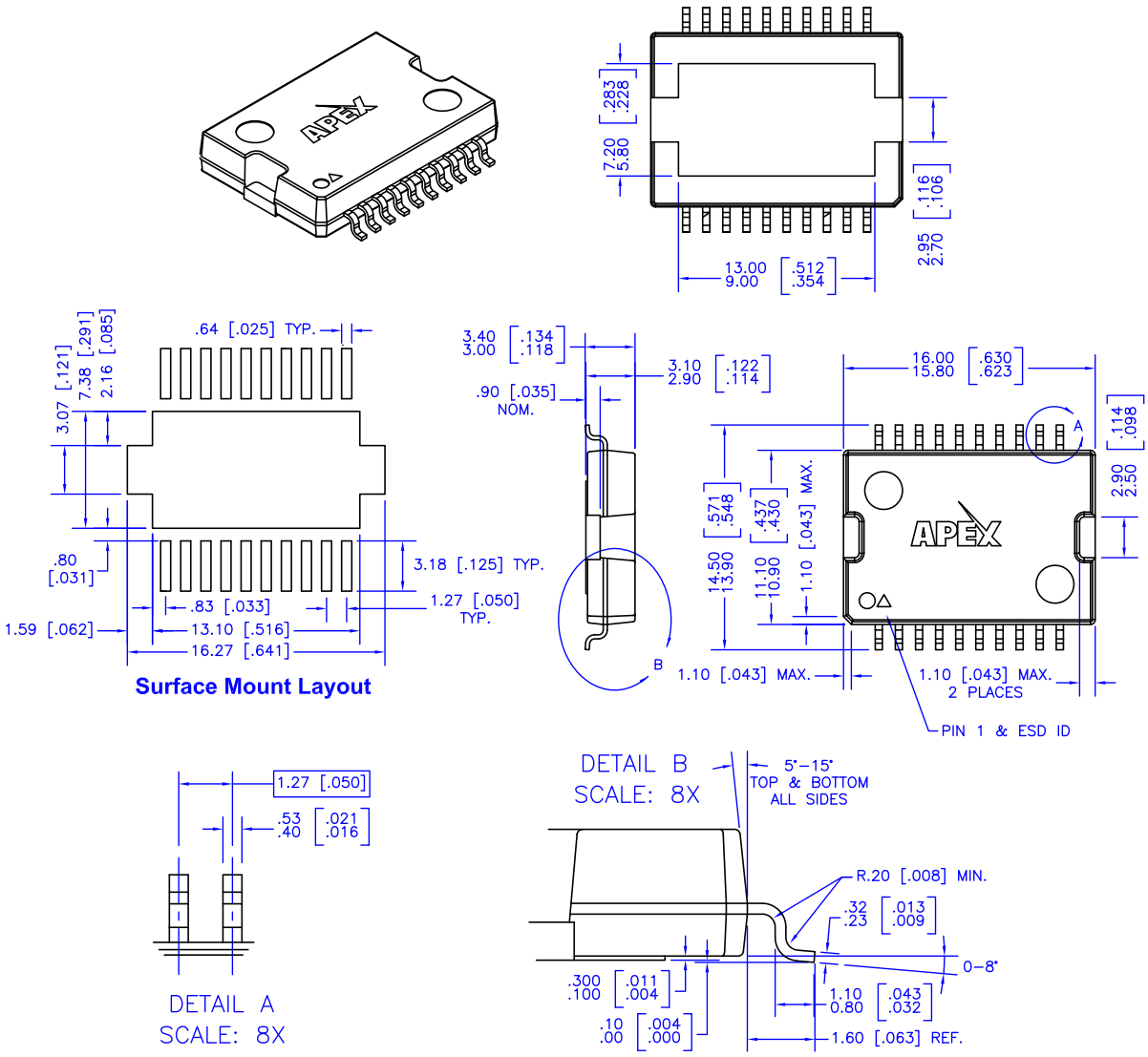
Like many high performance MOSFET amplifiers, the PA79 very sensitive to damage due to electrostatic discharge (ESD). Failure to follow proper ESD handling procedures could have results ranging from reduced operating performance to catastrophic damage. Minimum proper handling includes the use of grounded wrist or shoe straps, grounded work surfaces. Ionizers directed at the work in progress can neutralize the charge build up in the work environment and are strongly recommended.

PACKAGE OPTIONS

Part Number	Apex Package Style	Description	MSL[1]
PA79DK	DK	20-pin PSOP	Level 3

1. The Moisture Sensitivity Level rating according to the JEDEC industry standard classification.

PACKAGE STYLE DK



NOTES:
1. Dimensions are millimeters & [inches].
2. Bracketed alternate units are for reference only.
3. Dimple on lid & ESD triangle denote pin 1.
4. Heat Slug: C10200 copper with Ni–Pd–Au plating
5. Lead frame: C19400 copper with SNi–Pd–Au plating.
6. Mold compound: MP–8000AN or EME6600HR epoxy
7. Package weight: .086 oz. [2.44 g]
8. Suggested surface mount layout for reference only.

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